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PCB

Compal Confidential

HM51_TR/HM70_TR Discrete

NDWG2/NDWH1 LA5992 Schematic Document

Mobile AMD S1G3/RS880M/SB710

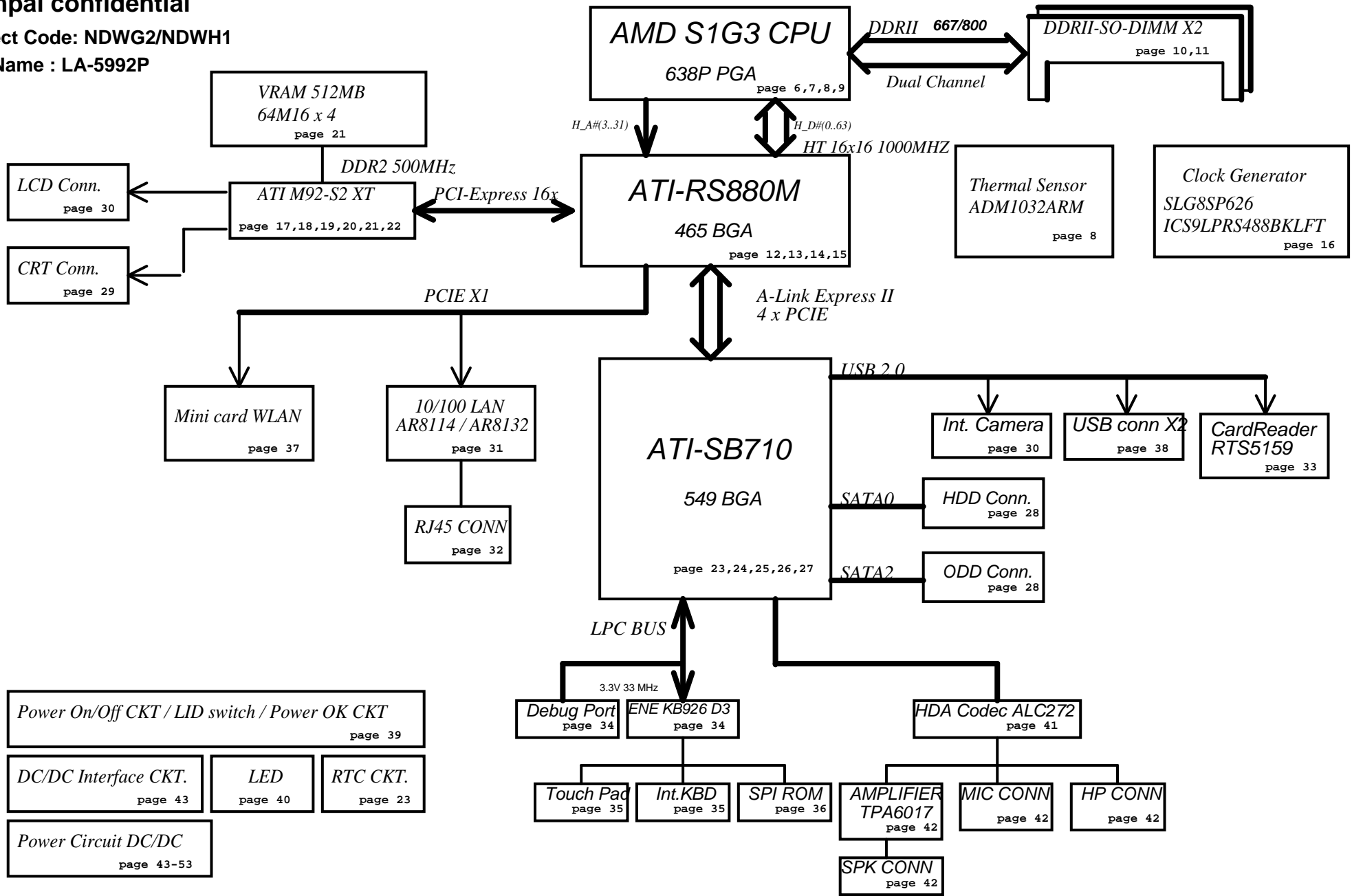
2009/12/02 Rev 1.0

Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>	
Issued Date	2009/09/25	Deciphered Date	2010/09/25	Title	SCHEMATIC MB A5992
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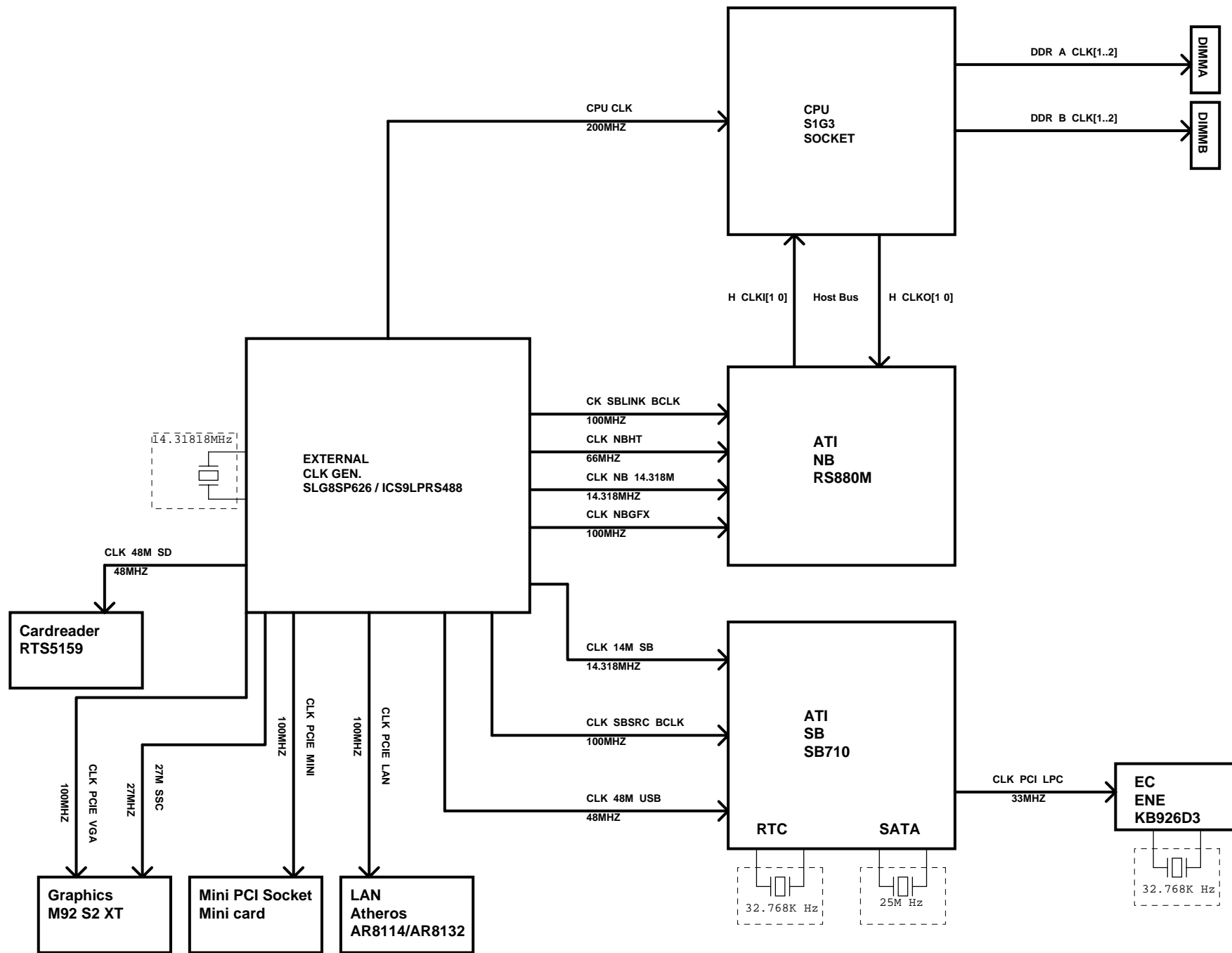
Compal confidential

Project Code: NDWG2/NDWH1

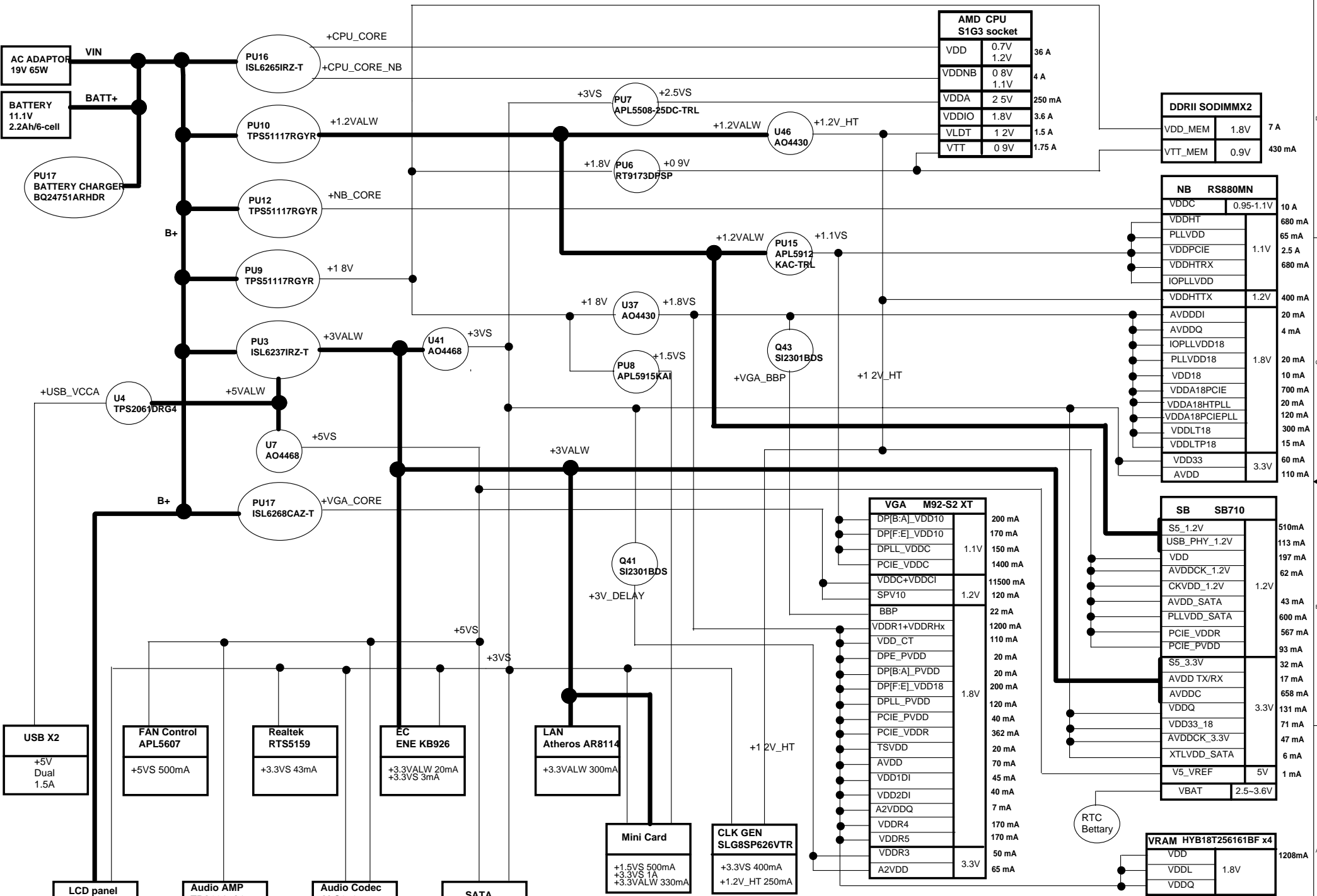
File Name : LA-5992P



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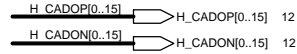
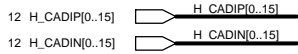


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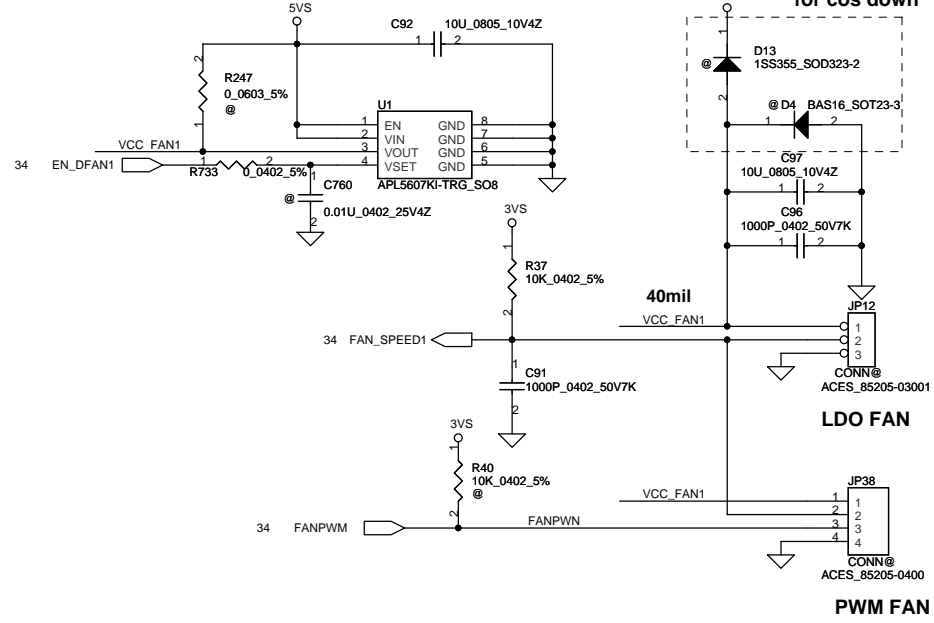
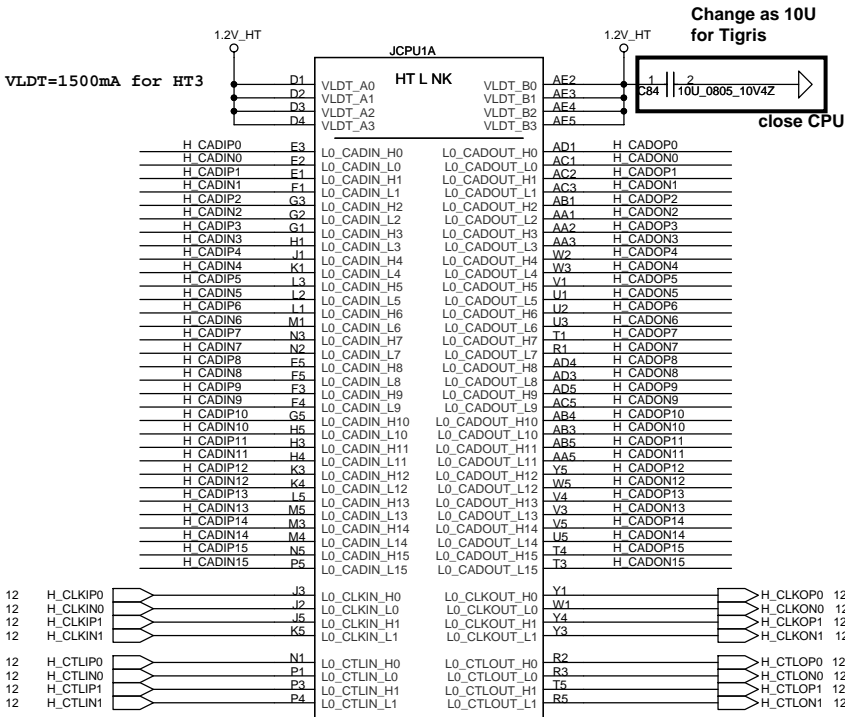


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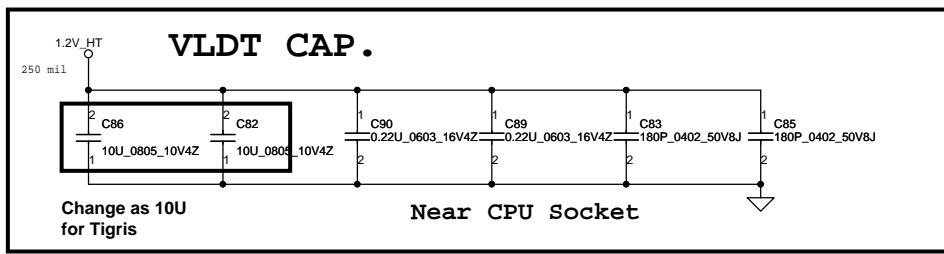
SCHEMATIC MB A5992



FAN Control Circuit

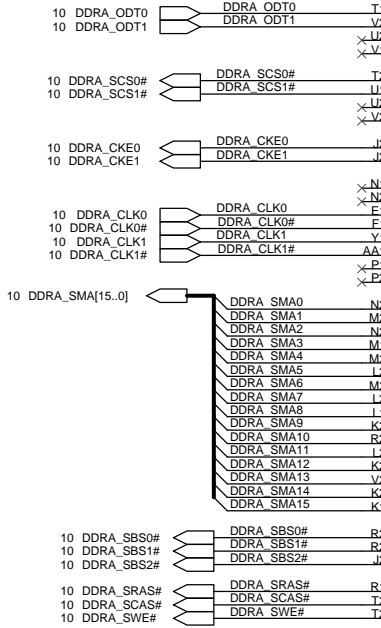
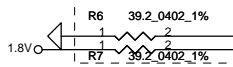


6090022100G_B
 Athlon 64 S1
 Processor Socket



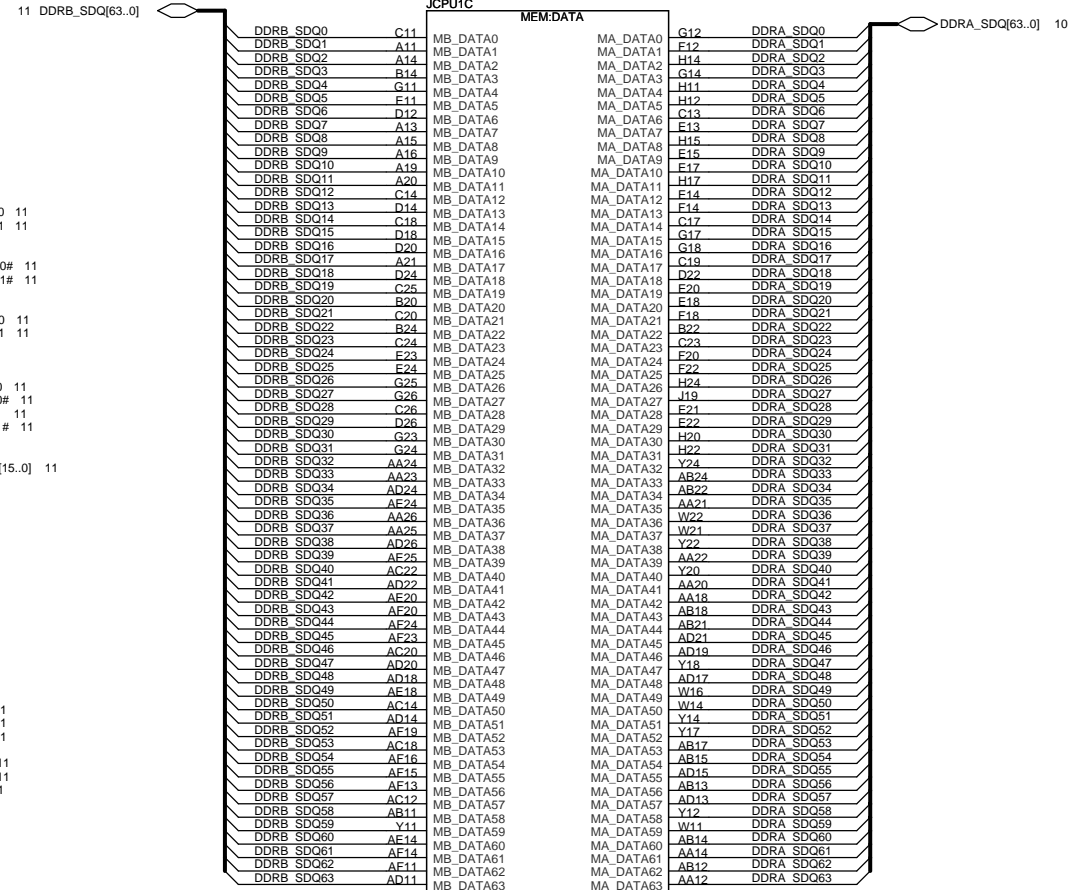
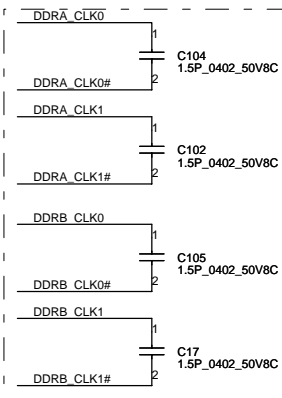
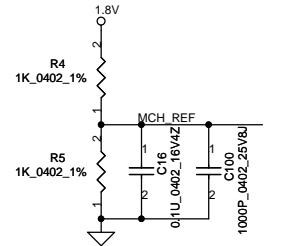
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Place them close to CPU within 1"



Athlon 64 S1 Processor Socket

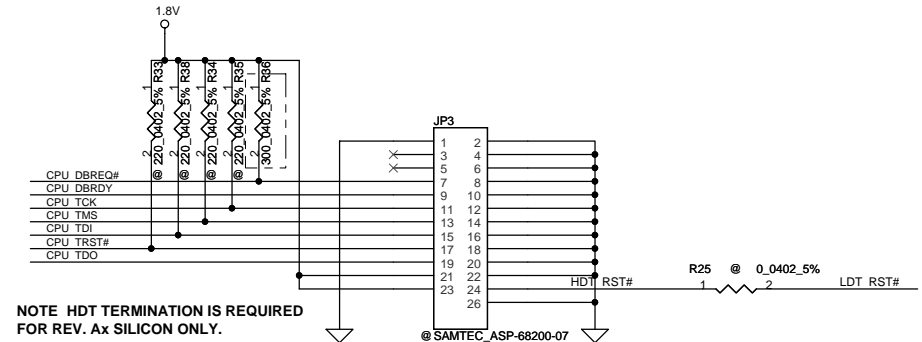
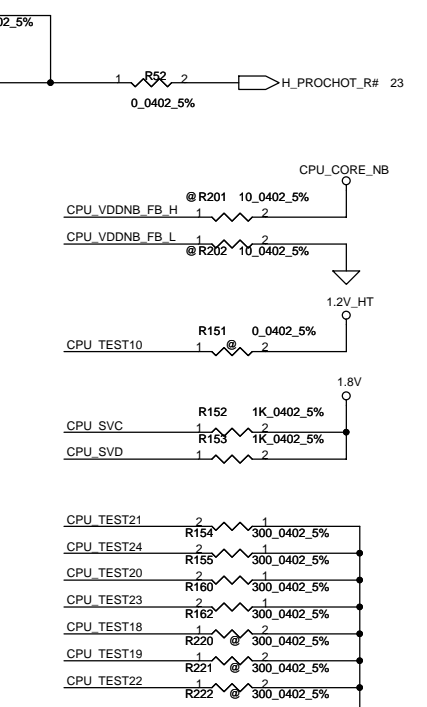
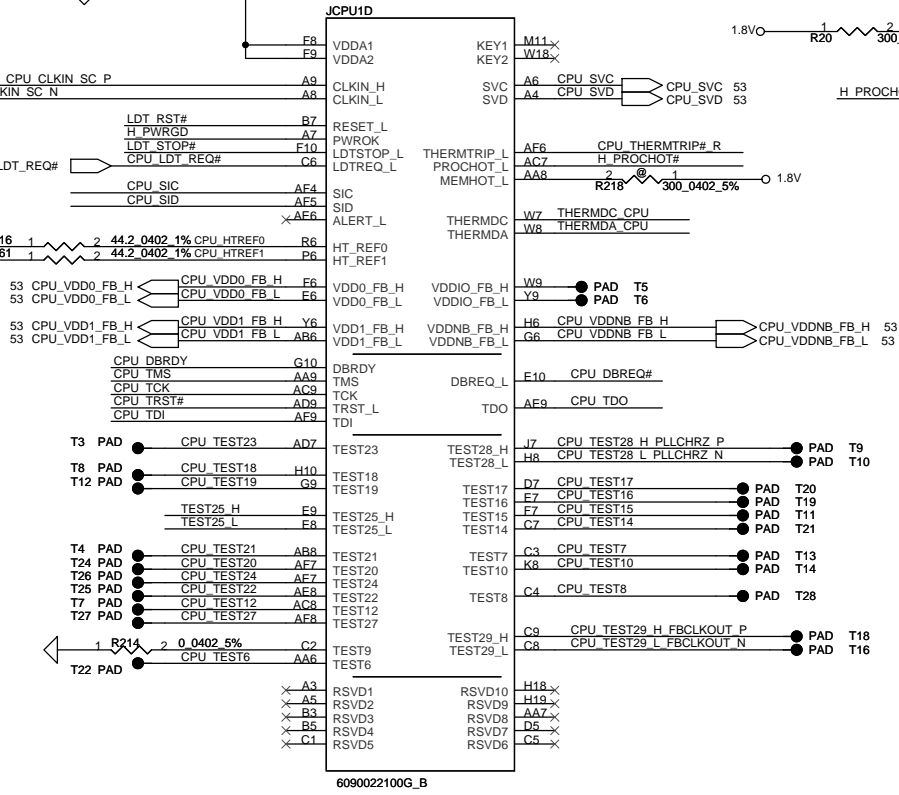
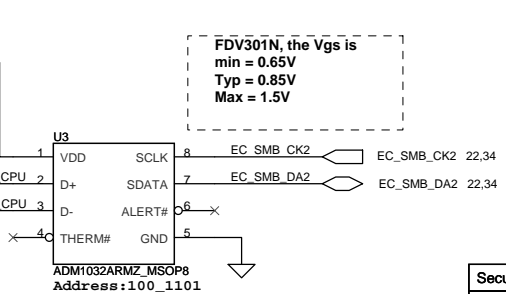
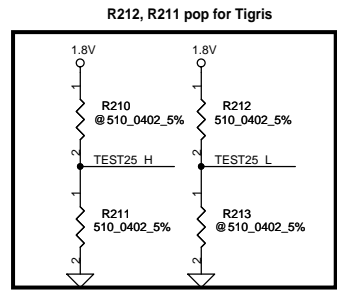
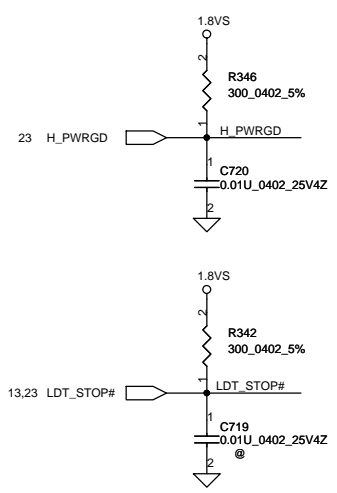
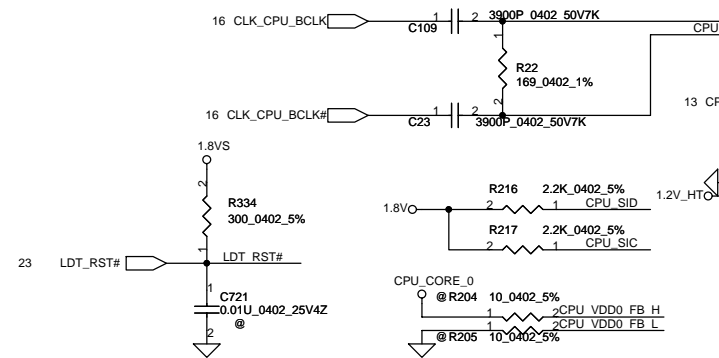
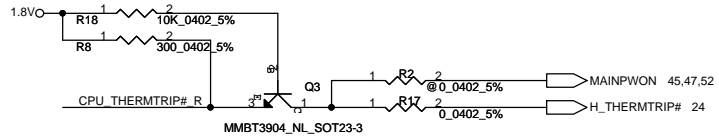
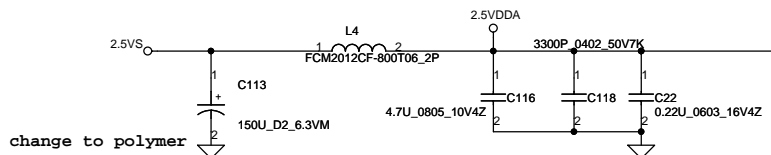
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



6090022100G_B Athlon 64 S1 Processor Socket

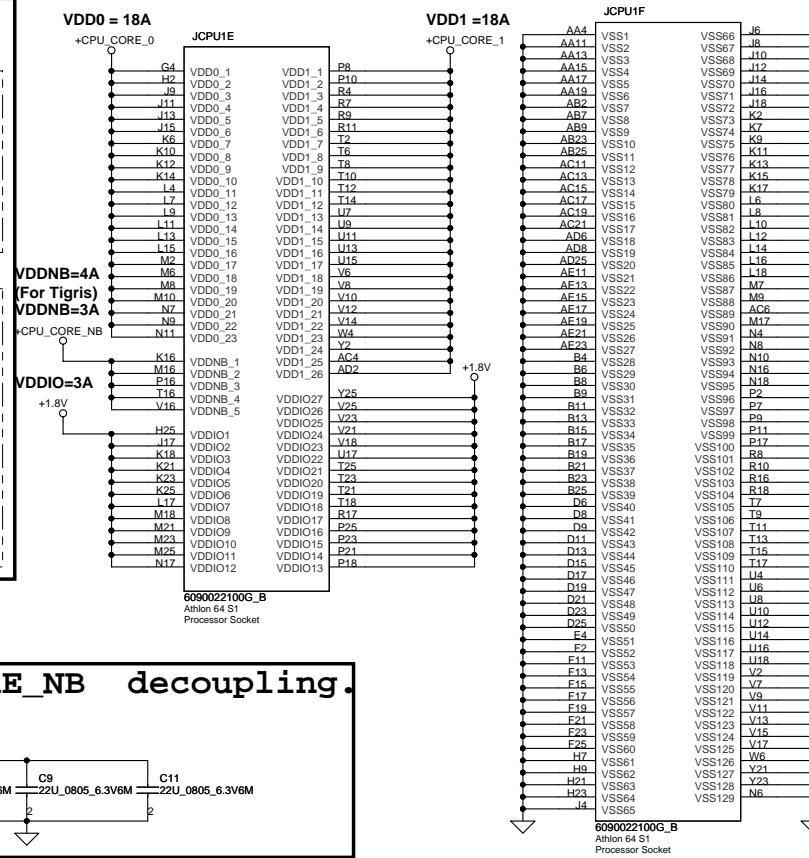
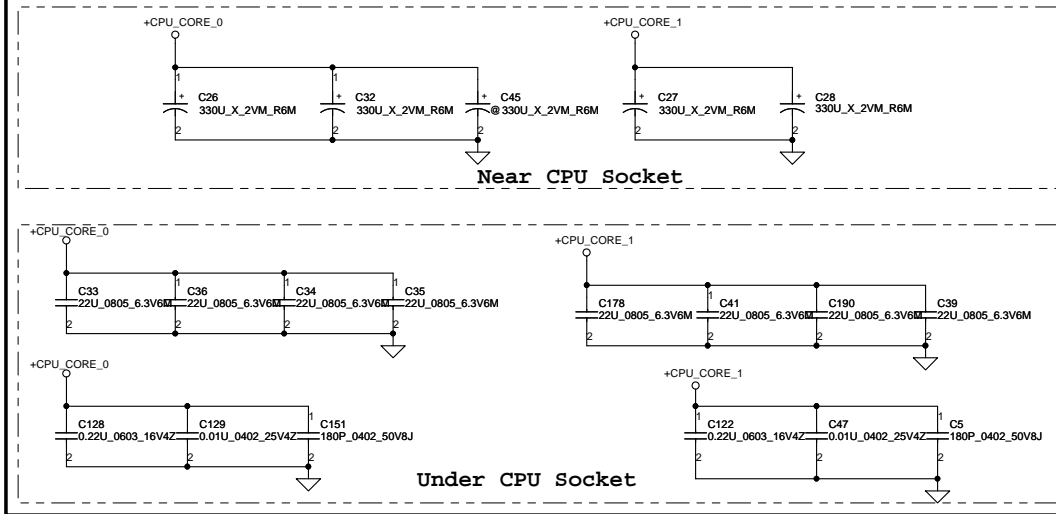
Processor DDR2 Memory Interface

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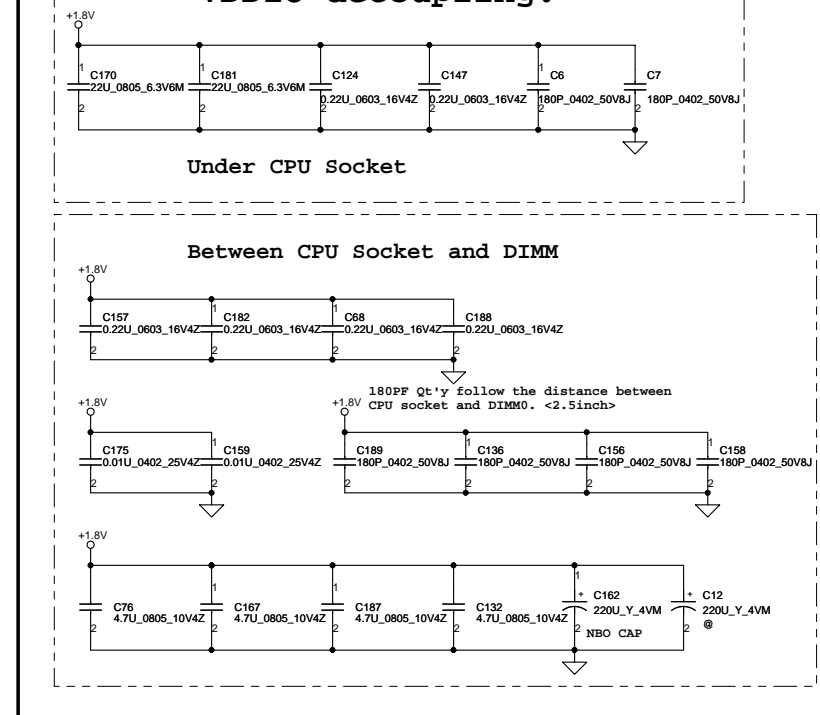


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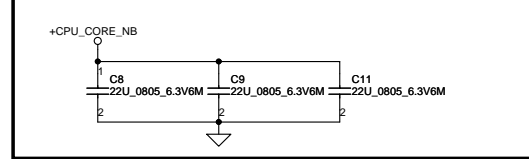
VDD(+CPU_CORE) decoupling.



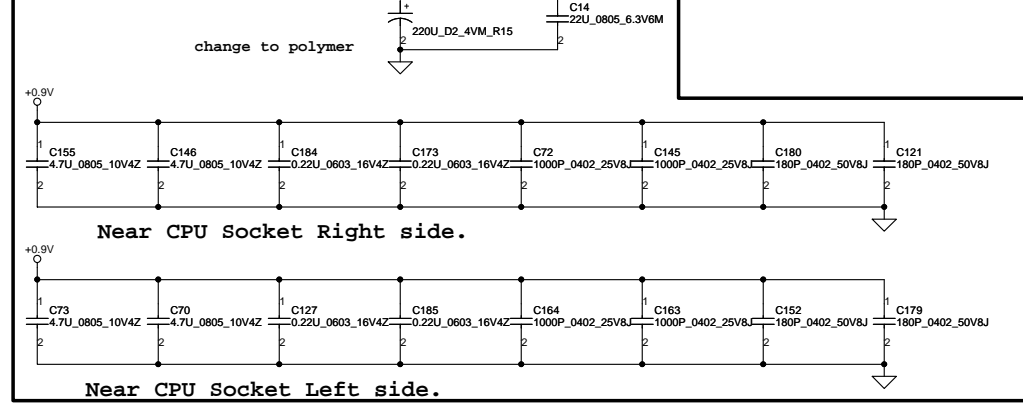
VDDIO decoupling.



+CPU_CORE_NB decoupling.

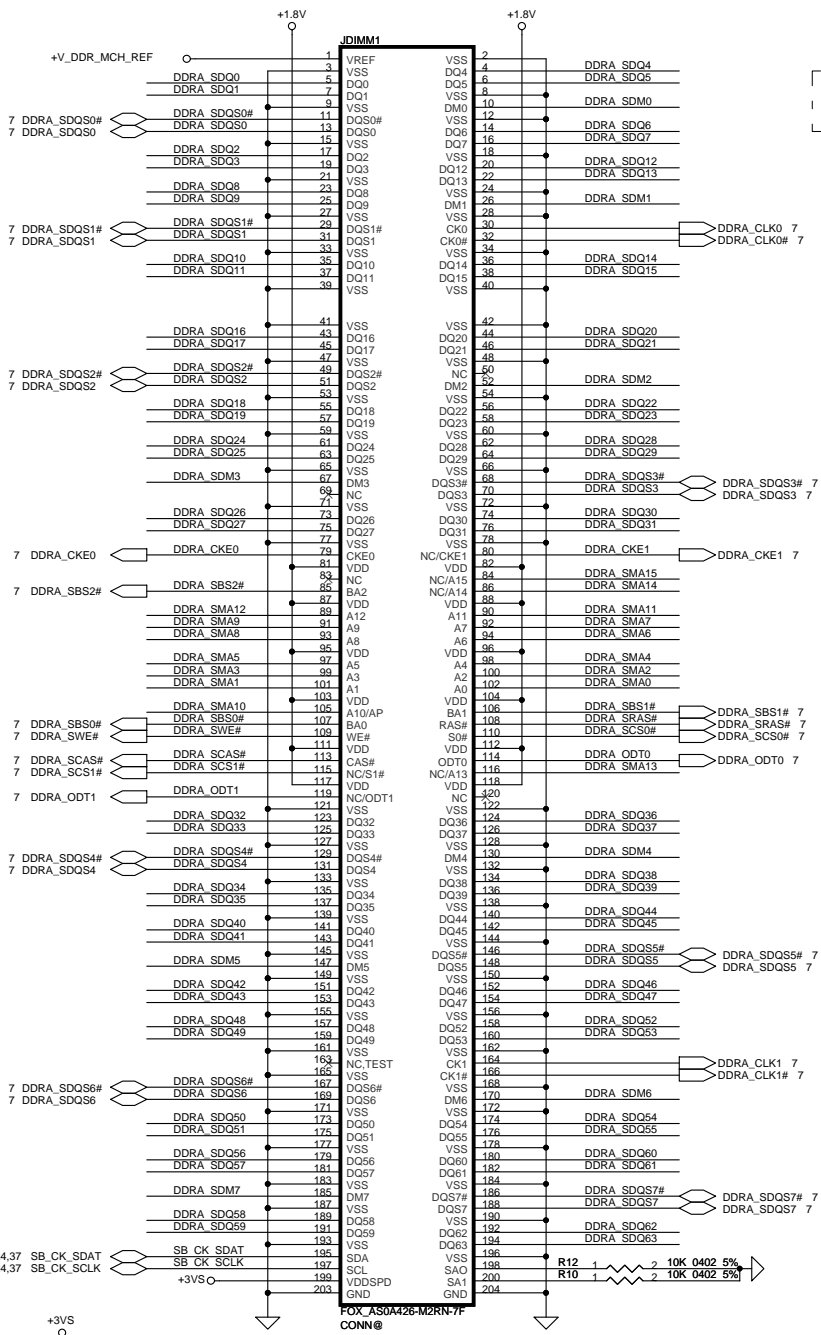
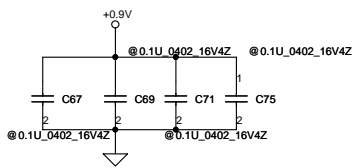
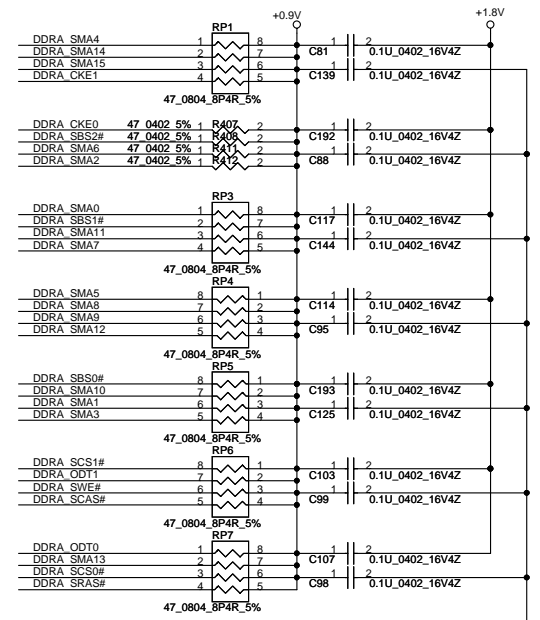
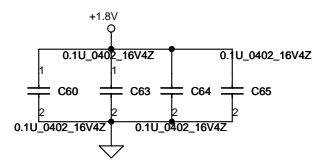
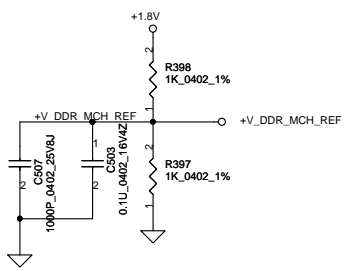


VTT decoupling.

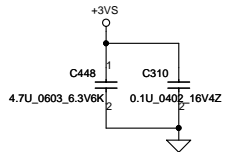


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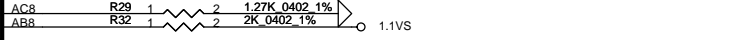
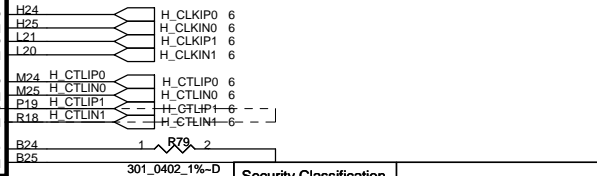
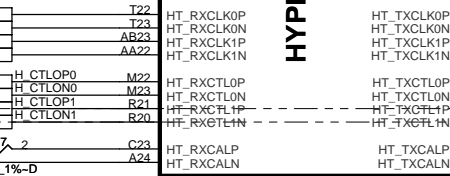
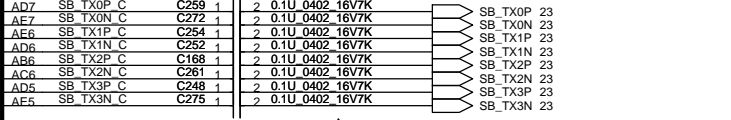
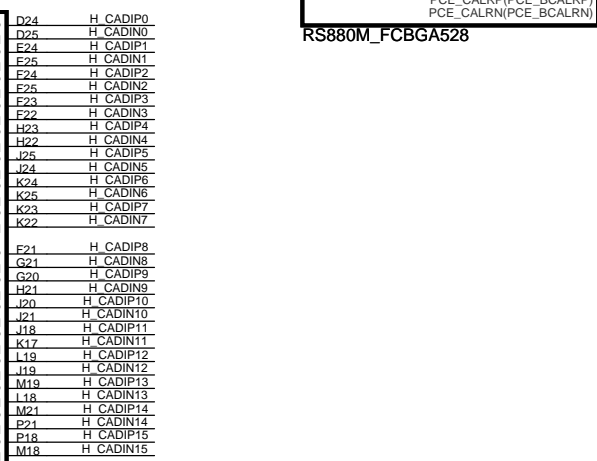
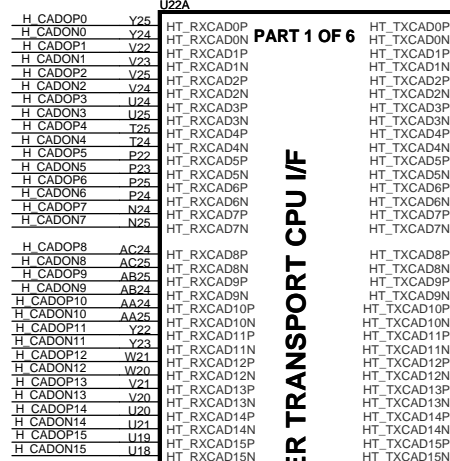
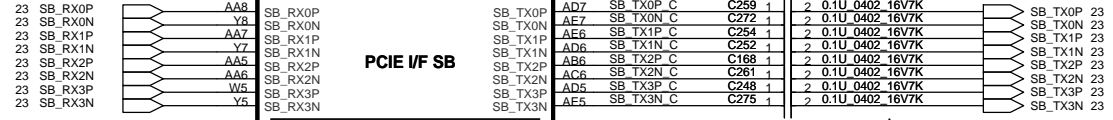
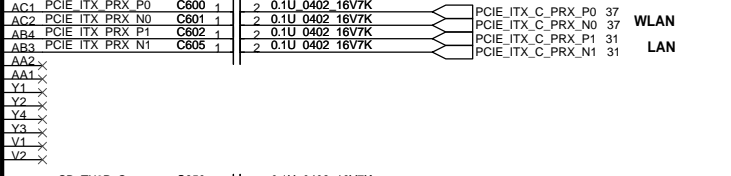
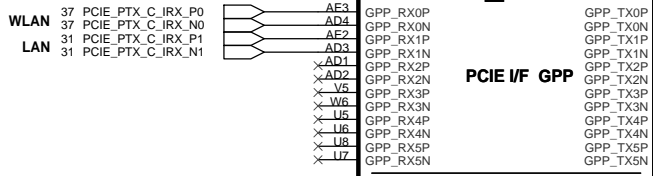
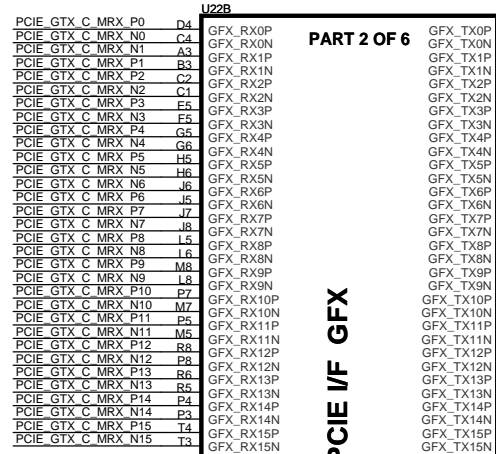
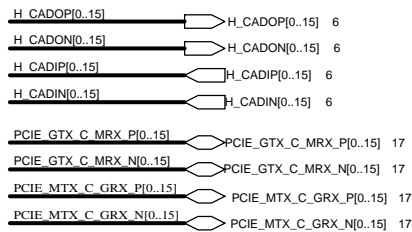
RESERVE
+V_DDR_MCH_REF BUFFER CIRCUIT



DIMM1 REV H:5.2mm (BOT)



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Place within 1" layout 4/8

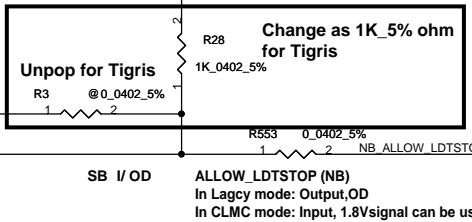
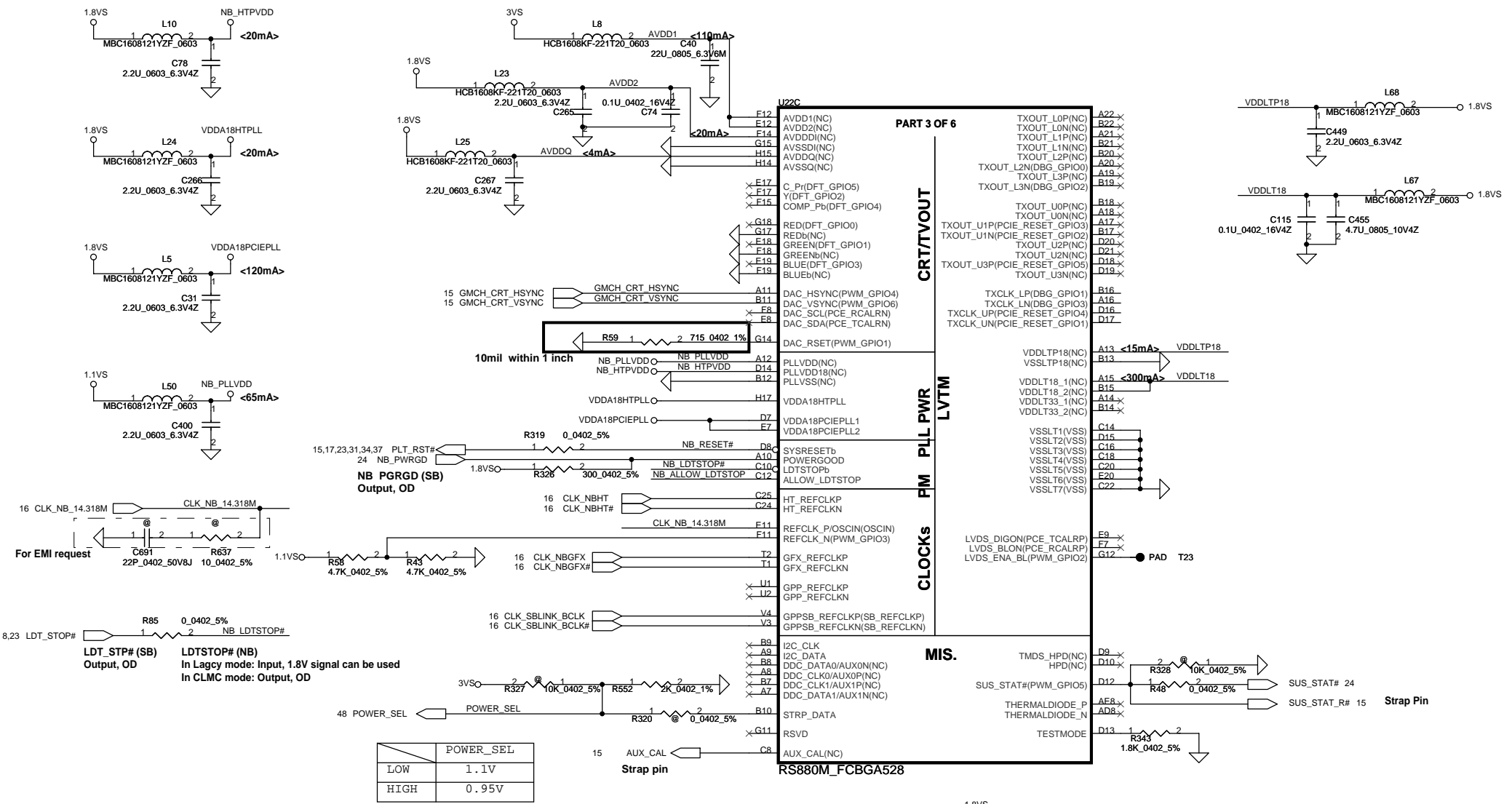
RS880M_FCBGA528

HT Link

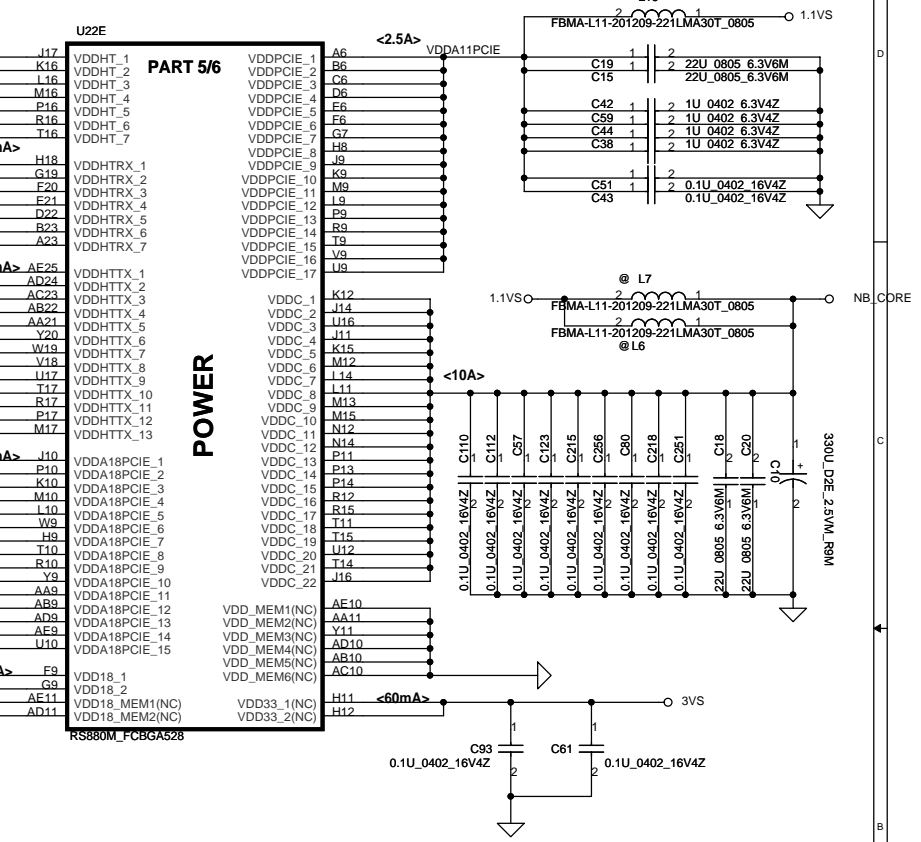
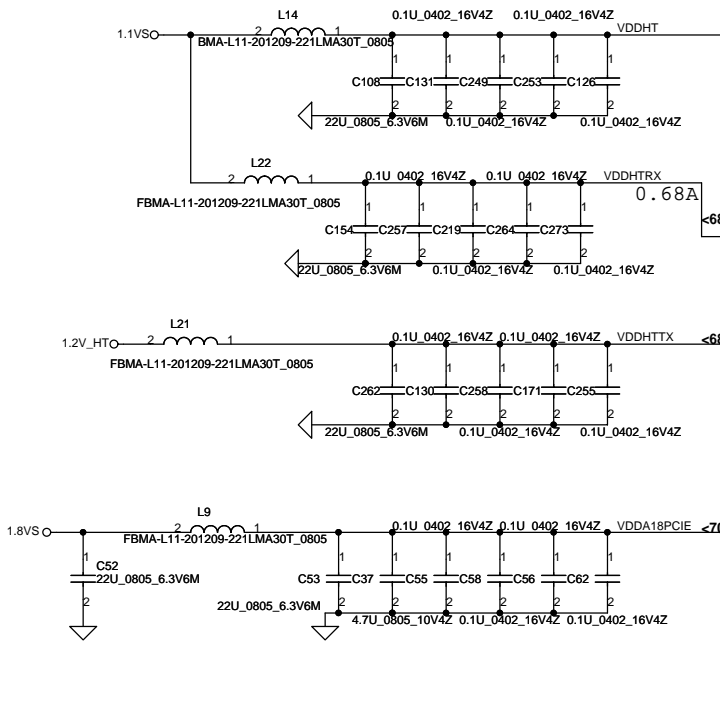
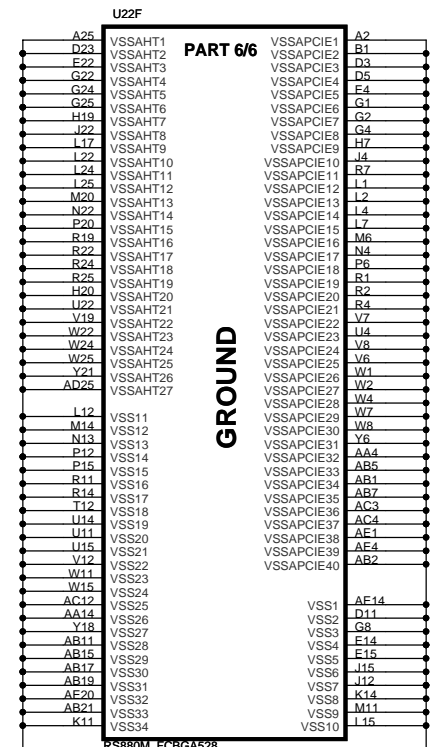
When tune trace length, must keep 1:4 on self-trace

Place within 1" layout 4/8

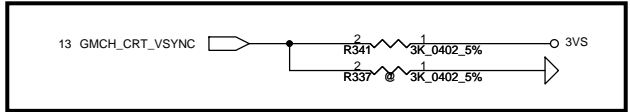
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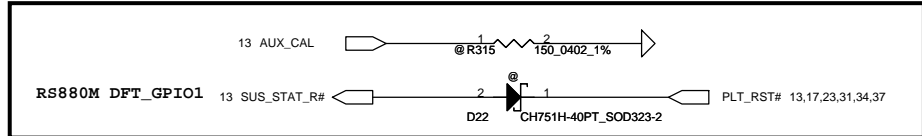


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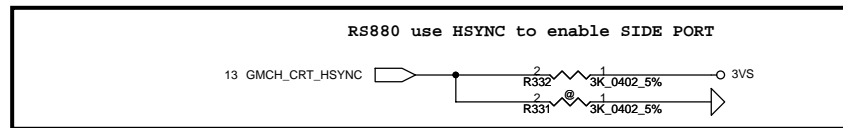
DFT GPIO5 STRAP DEBUG BUS GPIO ENABLEd

Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable (RS880)
 0 : Enable (Rs880)



DFT GPIO1 LOAD EEPROM STRAPS

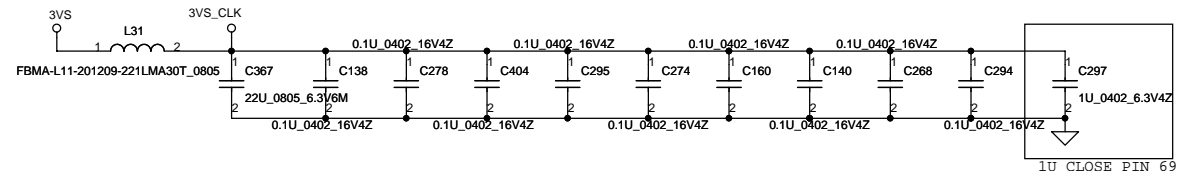
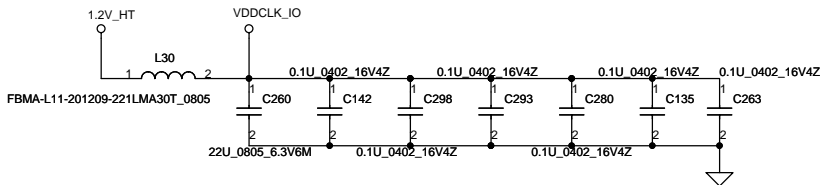
Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780/RS880M: DFT_GPIO1 RS880M:SUS_STAT



RS880 use HSYNC to enable SIDE PORT

RS740/RS780/RS880M: Enables Side port memory (RS880M use HSYNC#)
 0 : Enable (RS880M)
 1 : Disable(RS880M)

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SEL_27M	1	configure as 27M and 27M_SS output
	0	configure as SRC_7 output
27M_SEL	1*	configure as 27M and 27M_SS output
	0	configure as SRC_7 output
		* default
SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output
		* default

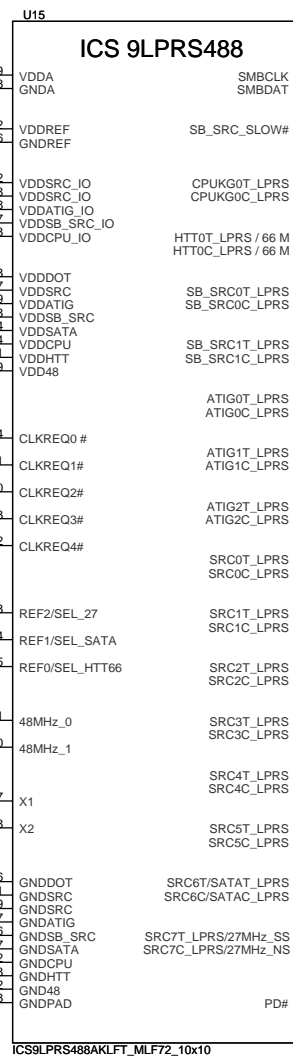
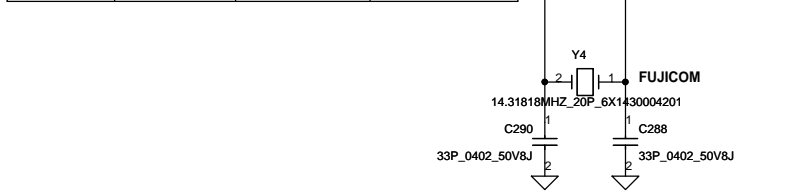
LAN request
31 LAN_CLKREQ#

MiniCard1 request
37 MINI1_CLKREQ#

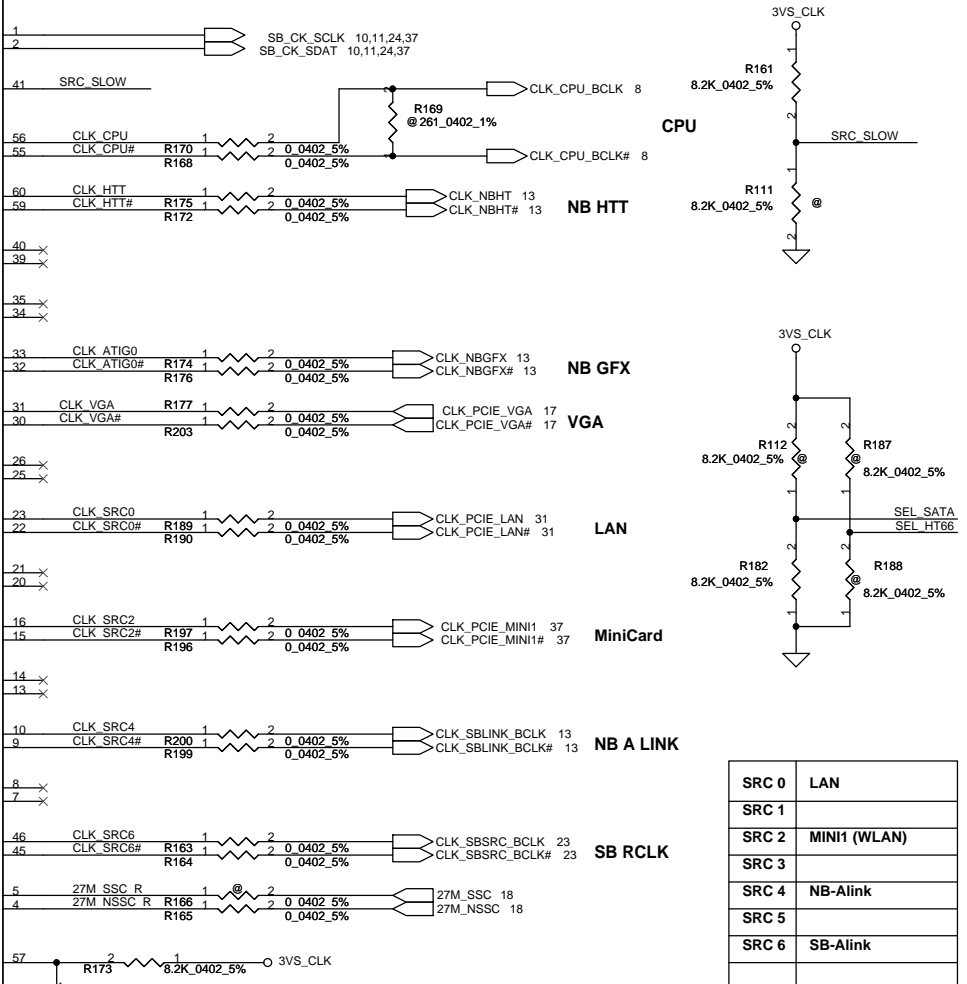
External 14MHz CLK for SB710
23 CLK_14M_SB

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	6M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF



ICS9LPRS488KLF72_10x10
Main--SLG8SP626VTR-SA00001Z310
Second--ICS9LPRS488CKLF72-SA000023H10

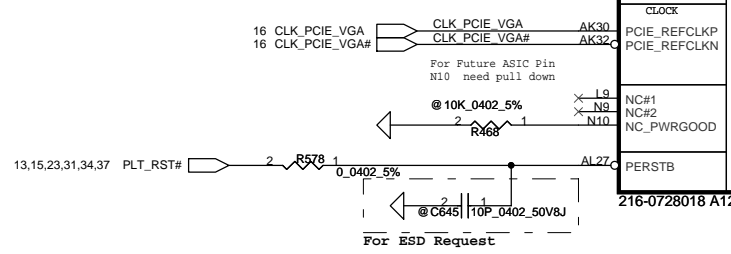
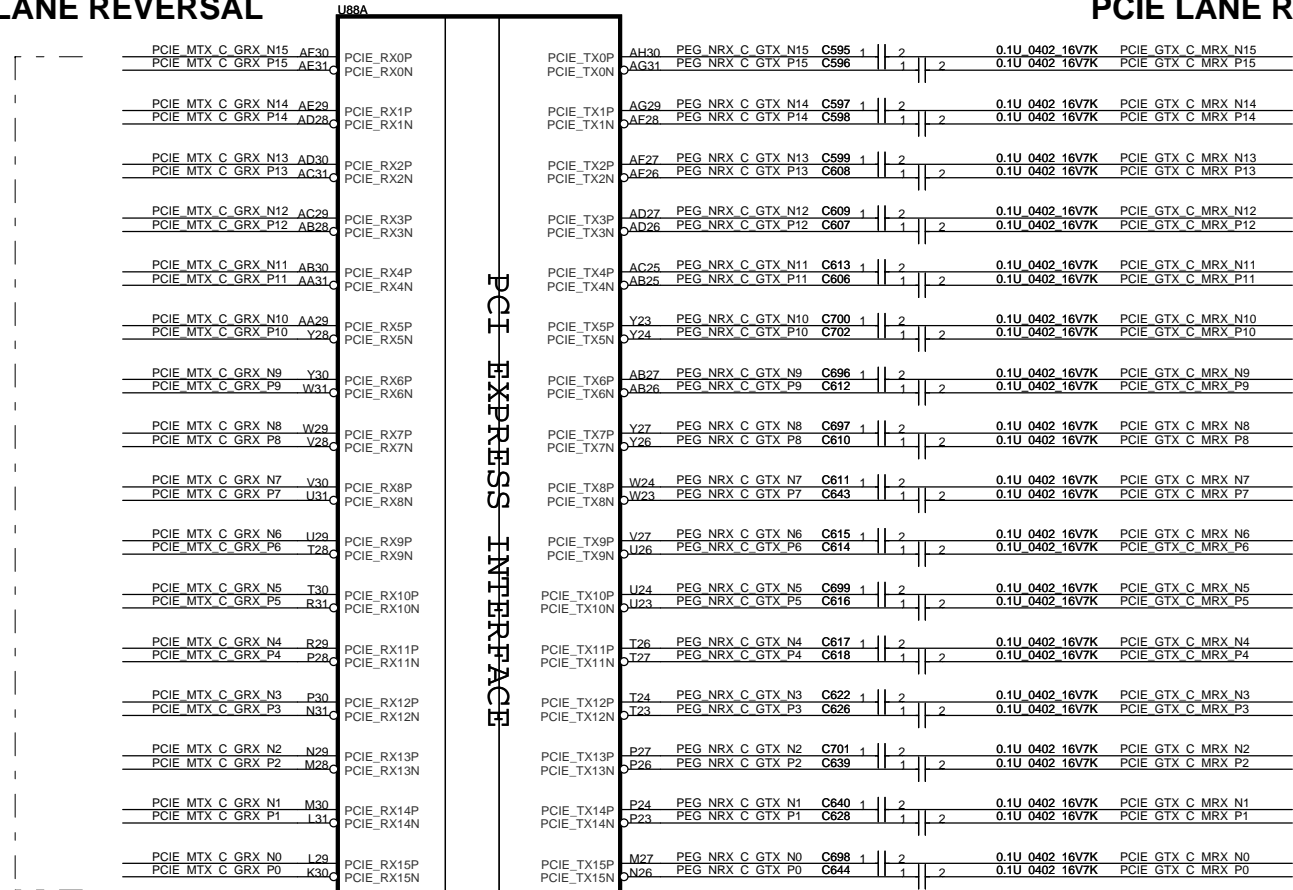
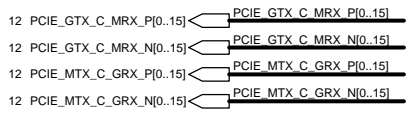


SRC 0	LAN
SRC 1	MINI1 (WLAN)
SRC 2	
SRC 3	
SRC 4	NB-Alink
SRC 5	
SRC 6	SB-Alink

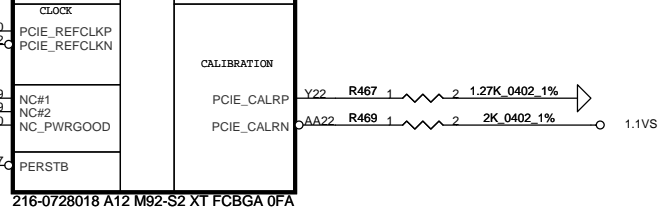
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PCIe LANE REVERSAL

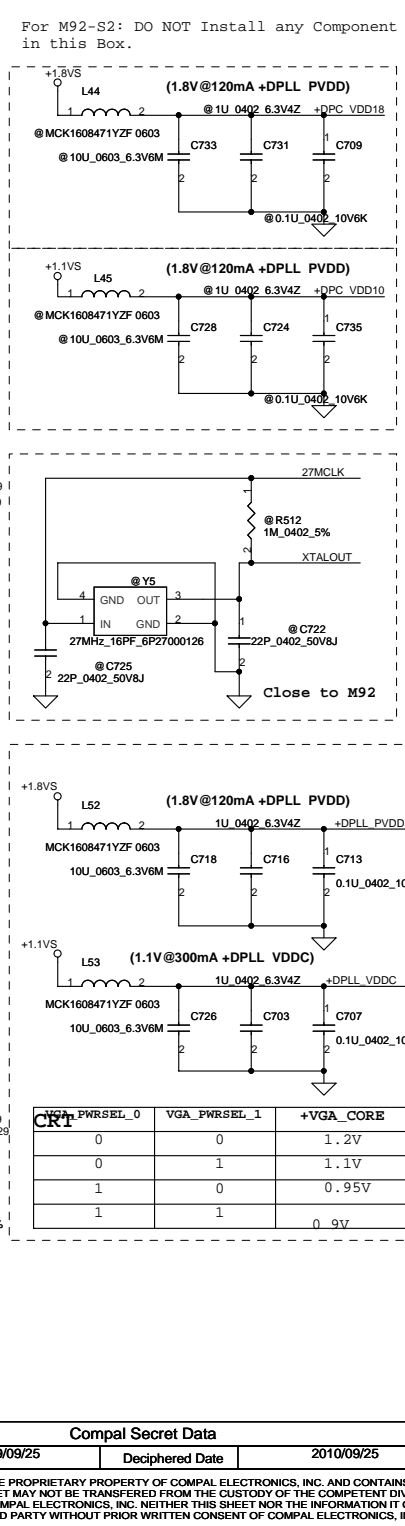
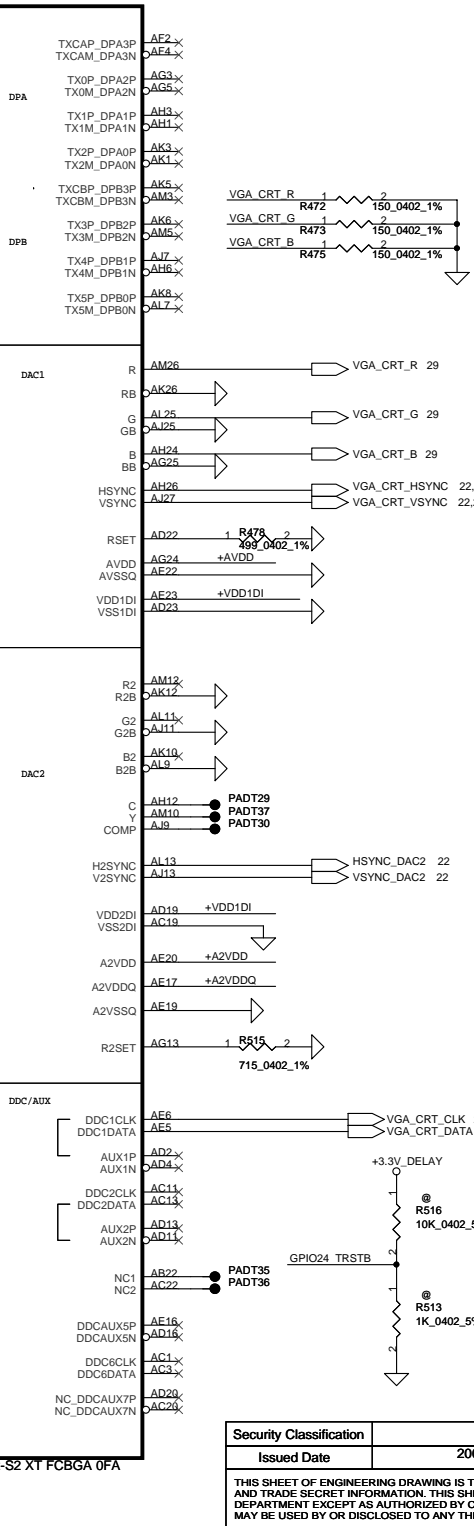
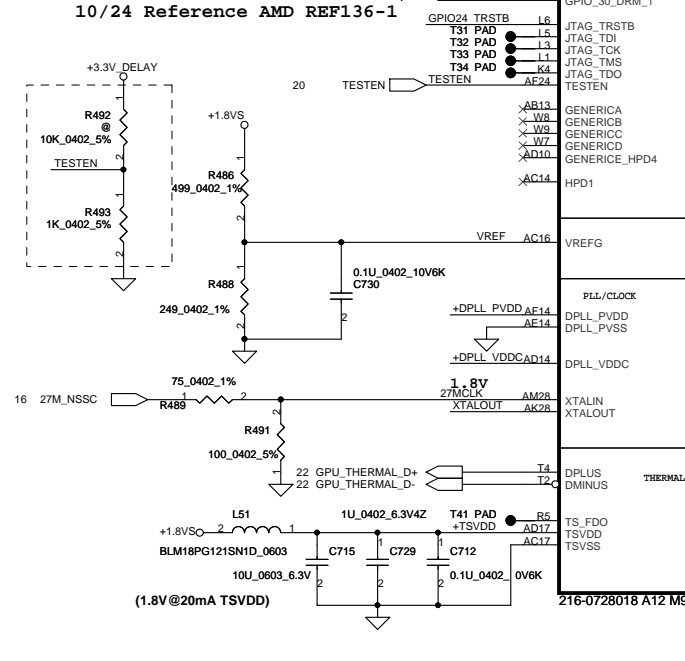
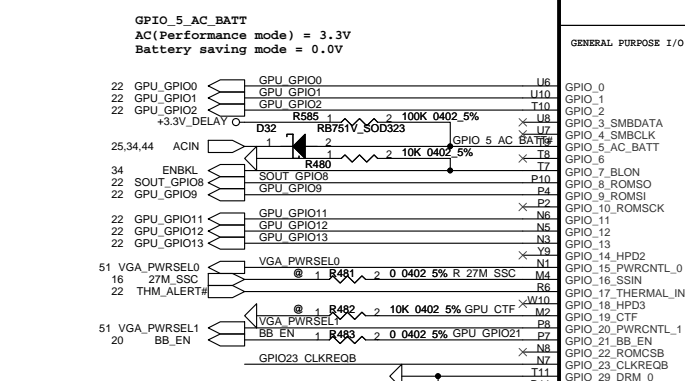
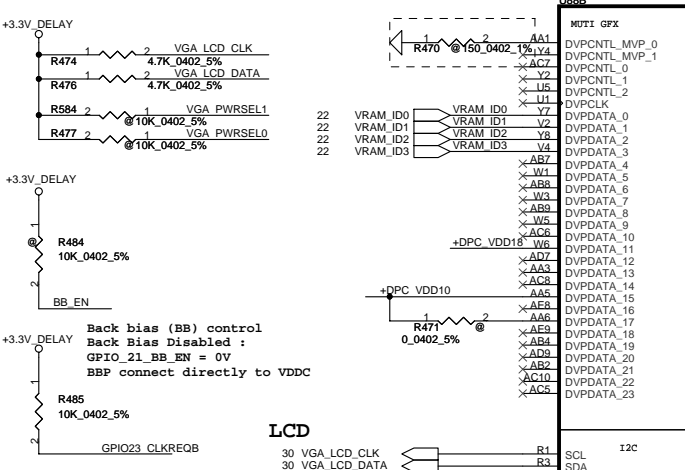
PCIe LANE REVERSAL



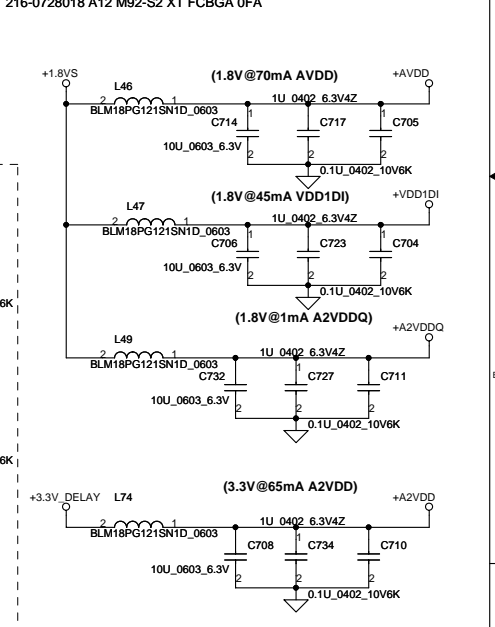
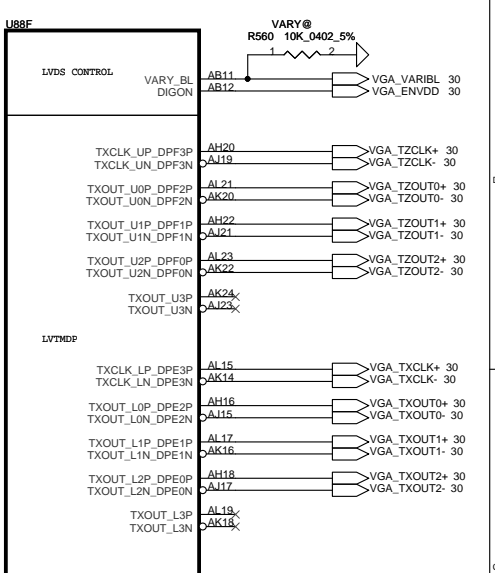
PCI EXPRESS INTERFACE



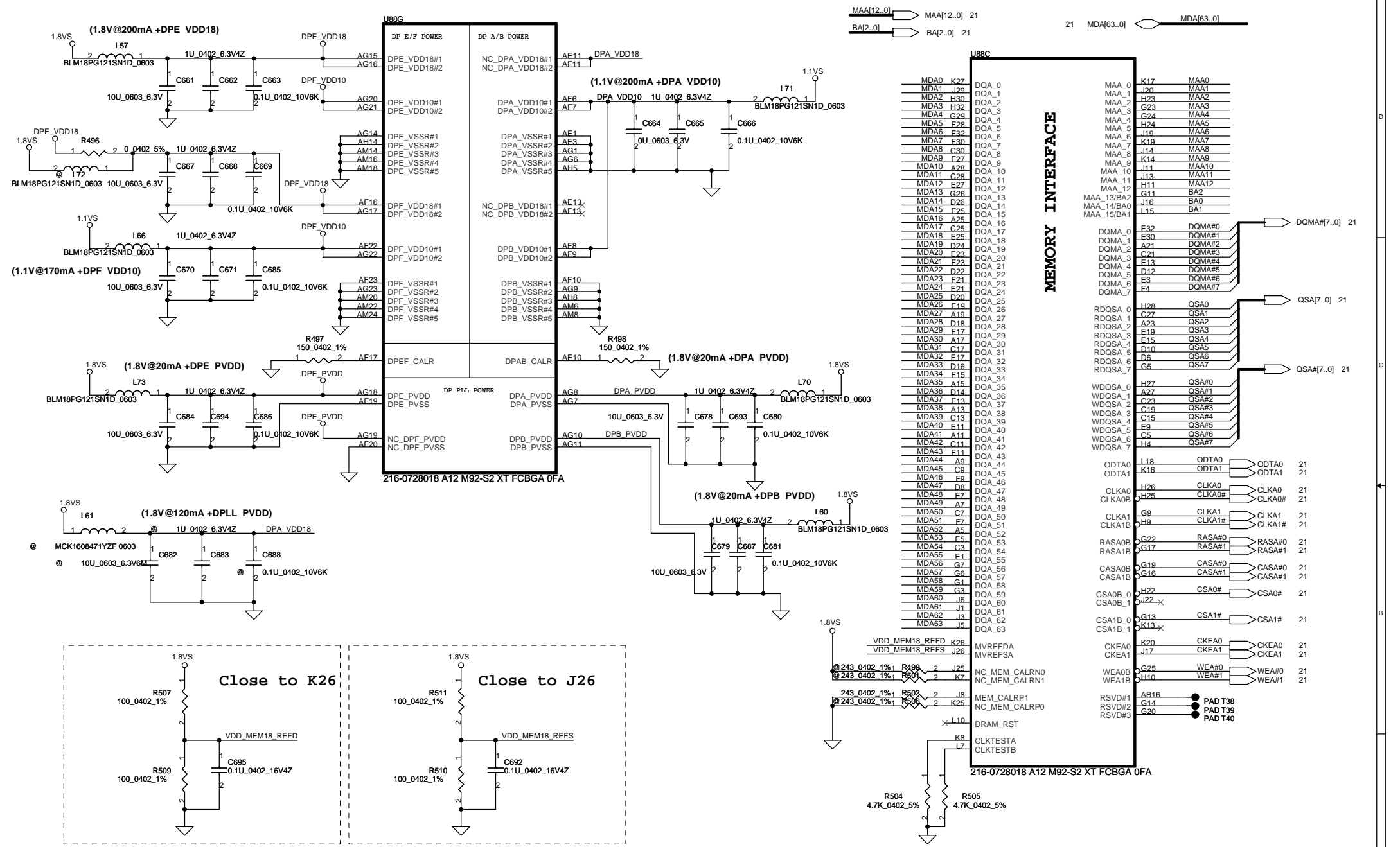
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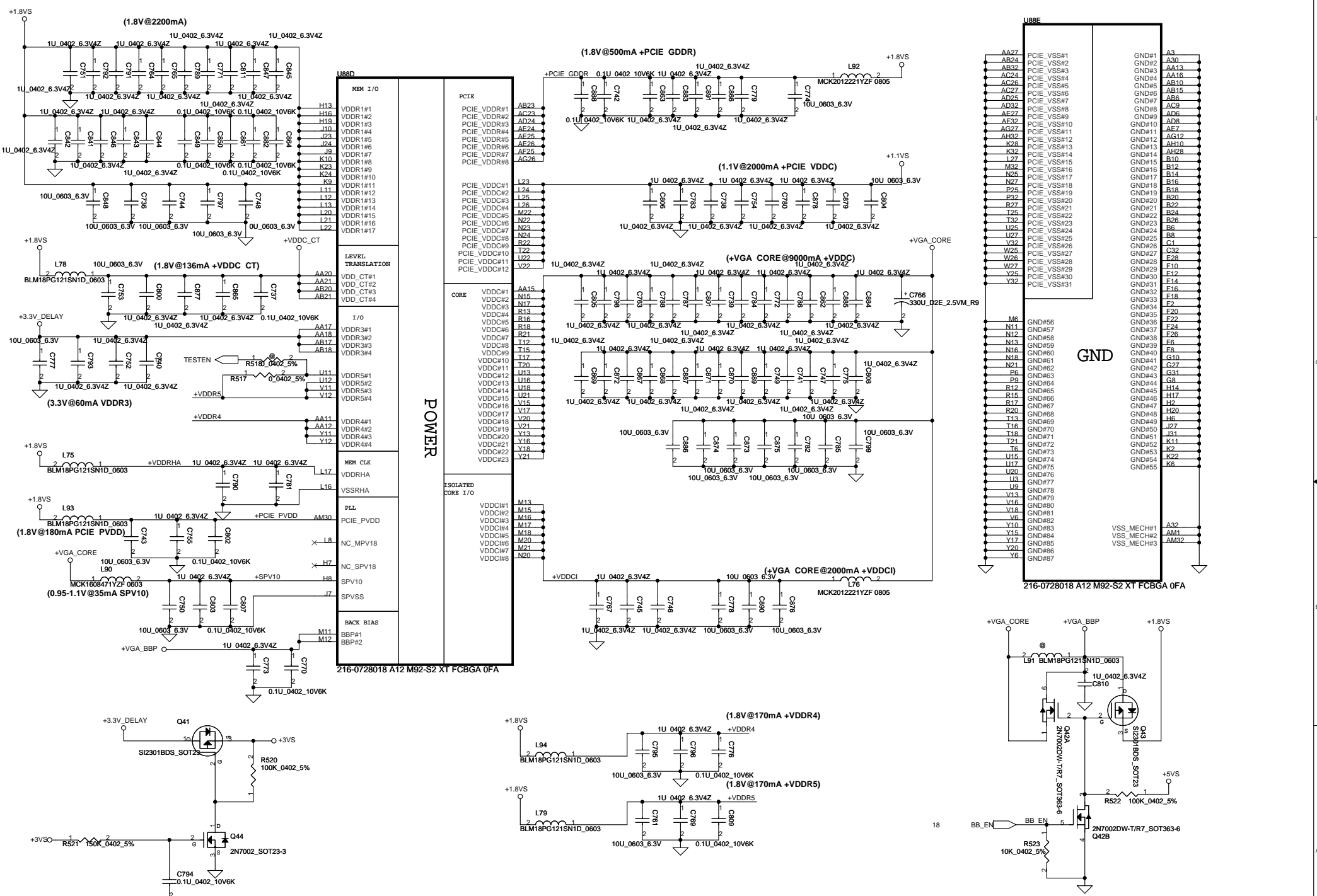
VGA_PWRSEL_0	VGA_PWRSEL_1	+VGA_CORE
0	0	1.2V
0	1	1.1V
1	0	0.95V
1	1	0.9V



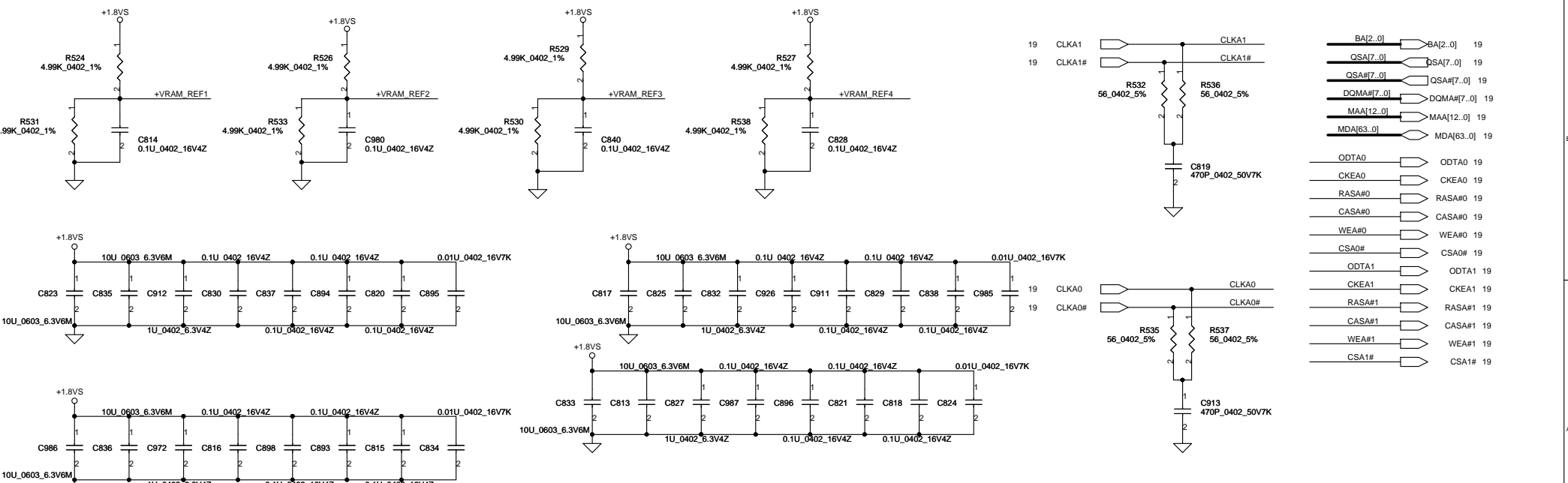
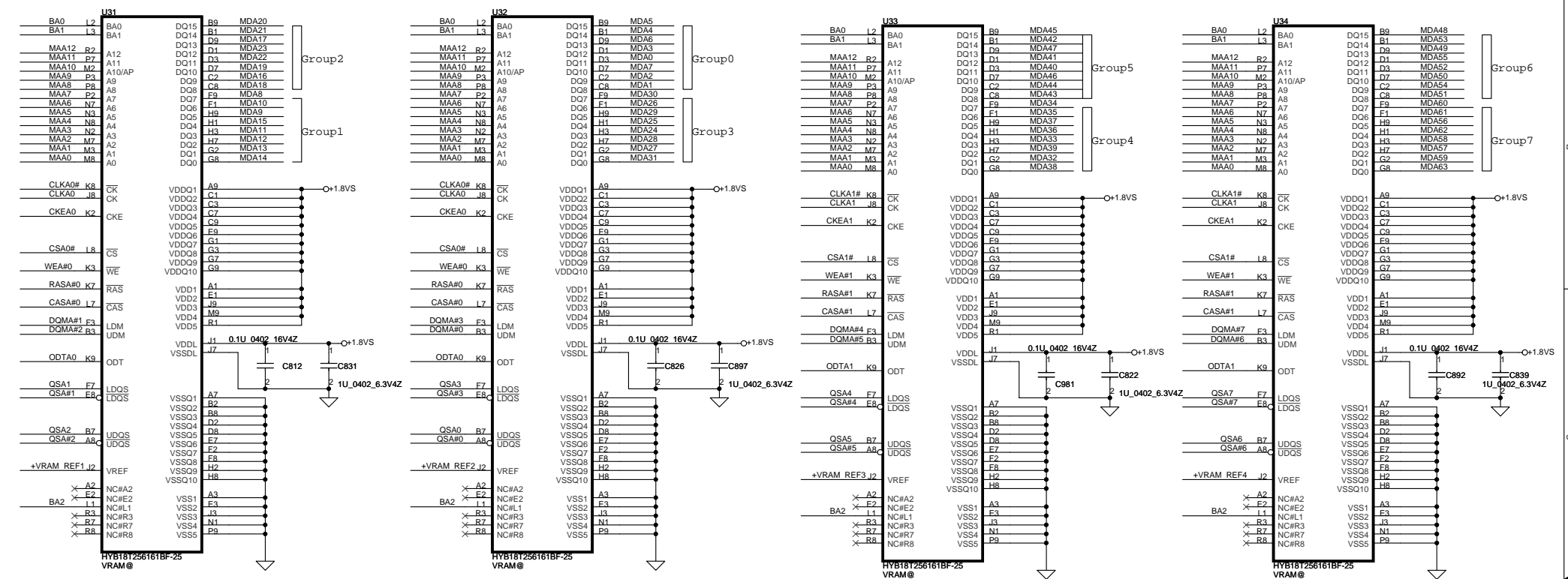
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Compal Electronics, Inc.

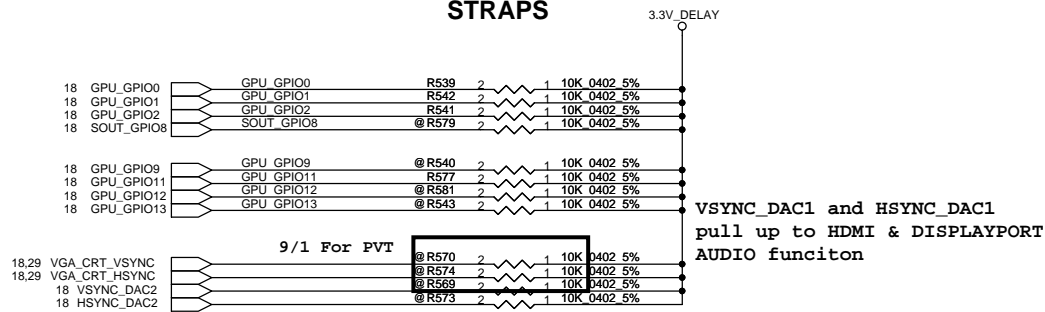
Schematic MB A5992

401836

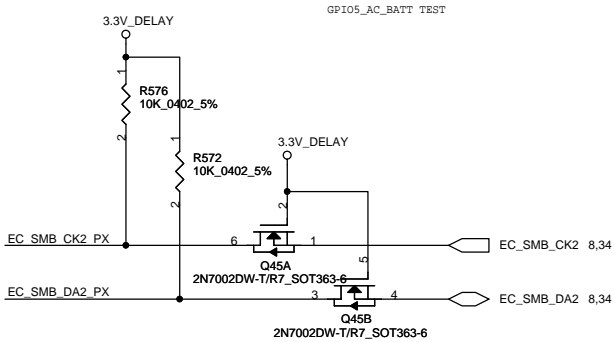
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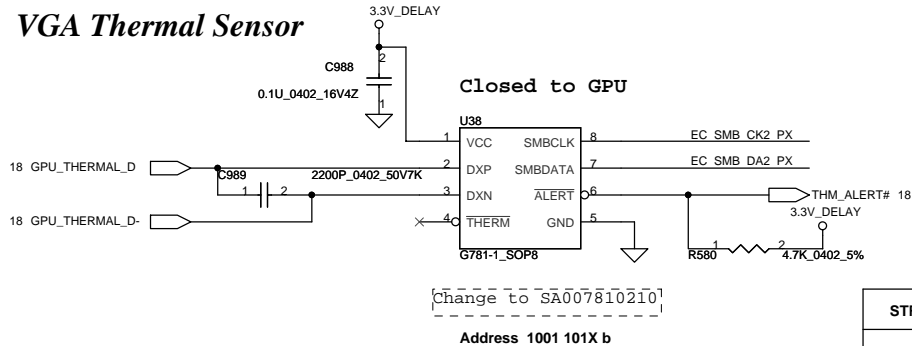
STRAPS



VSYNC_DAC1 and HSYNC_DAC1
pull up to HDMI & DISPLAYPORT
AUDIO function

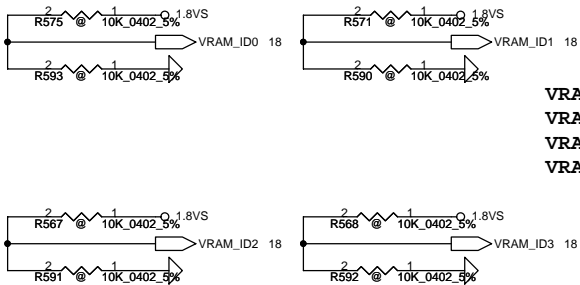


VGA Thermal Sensor



[change to SA007810210]

Address 1001 101X b



VRAM_ID0=VRAM_ID0_0
VRAM_ID1=VRAM_ID1_1
VRAM_ID2=VRAM_ID2_2
VRAM_ID3=VRAM_ID3_3

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMIDCFG(2,0)	GPIO[13:11]	BIF_RX_PLL_CALIB_BP	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HARD	H2SYNC	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X
AUD[0]	VSYNC		

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

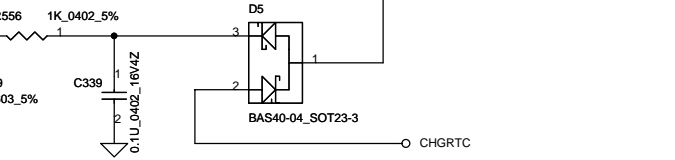
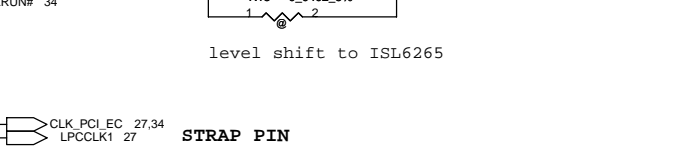
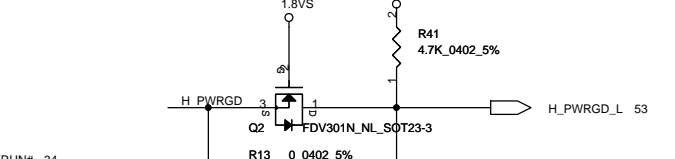
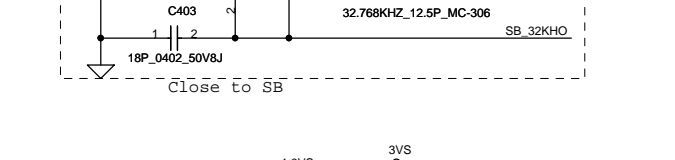
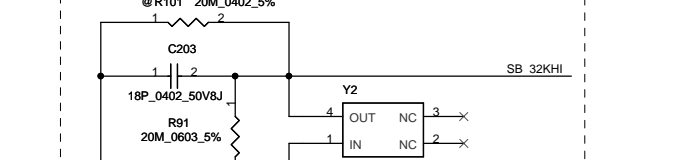
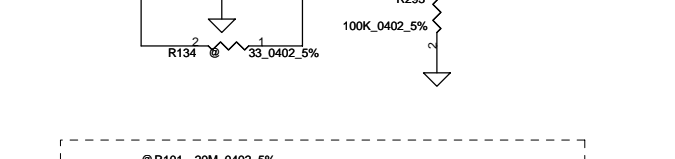
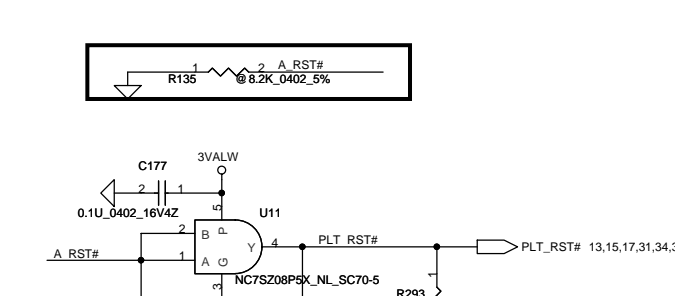
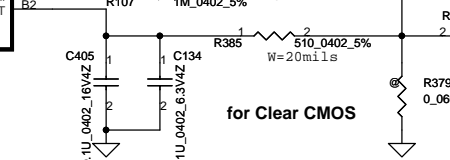
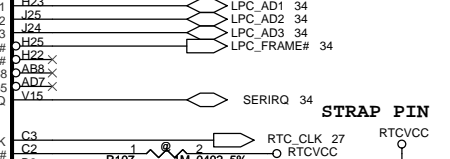
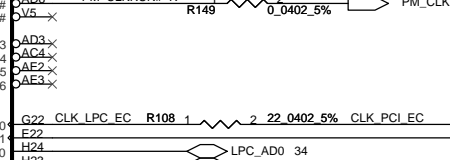
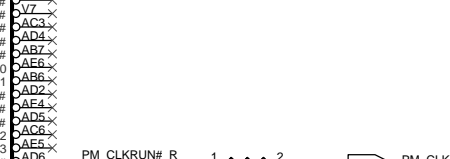
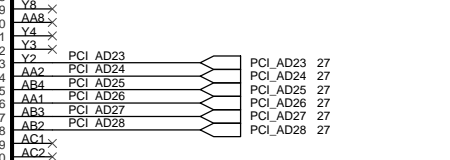
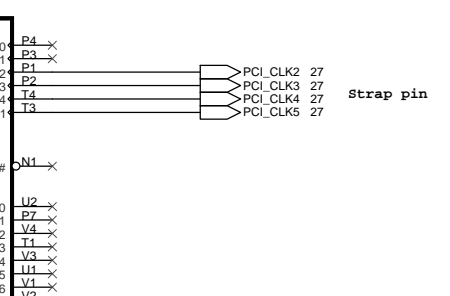
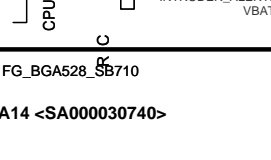
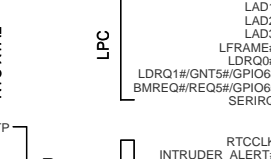
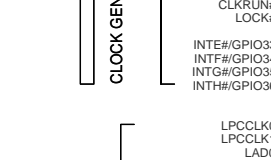
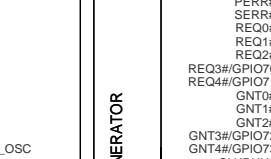
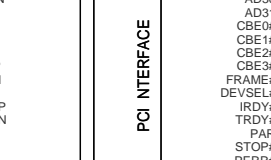
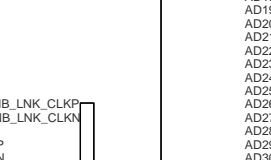
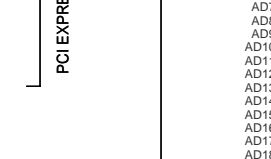
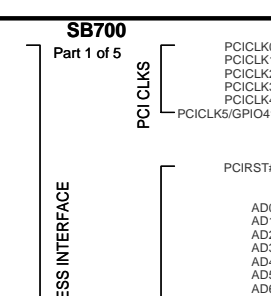
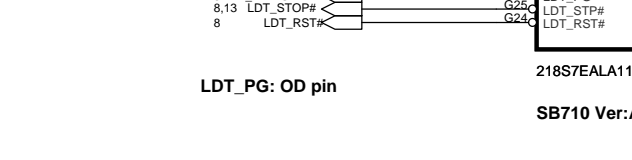
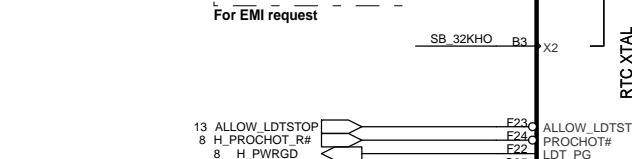
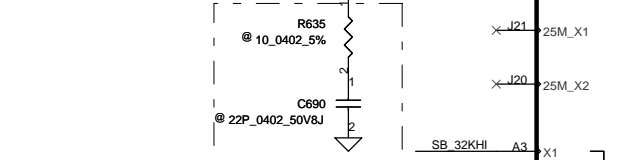
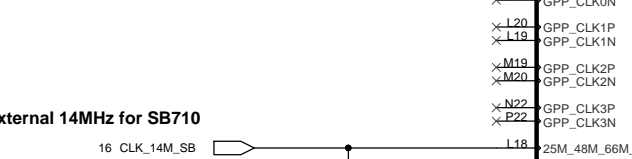
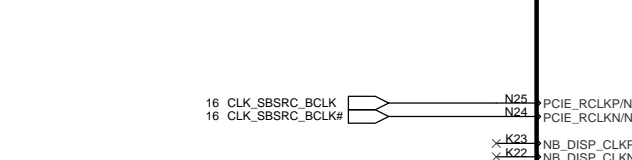
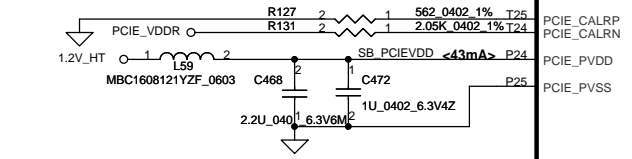
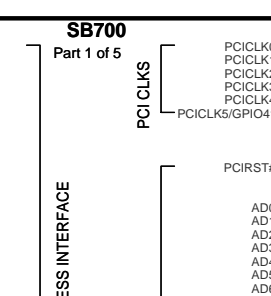
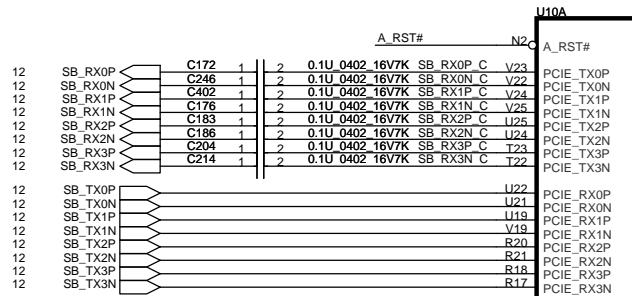
H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

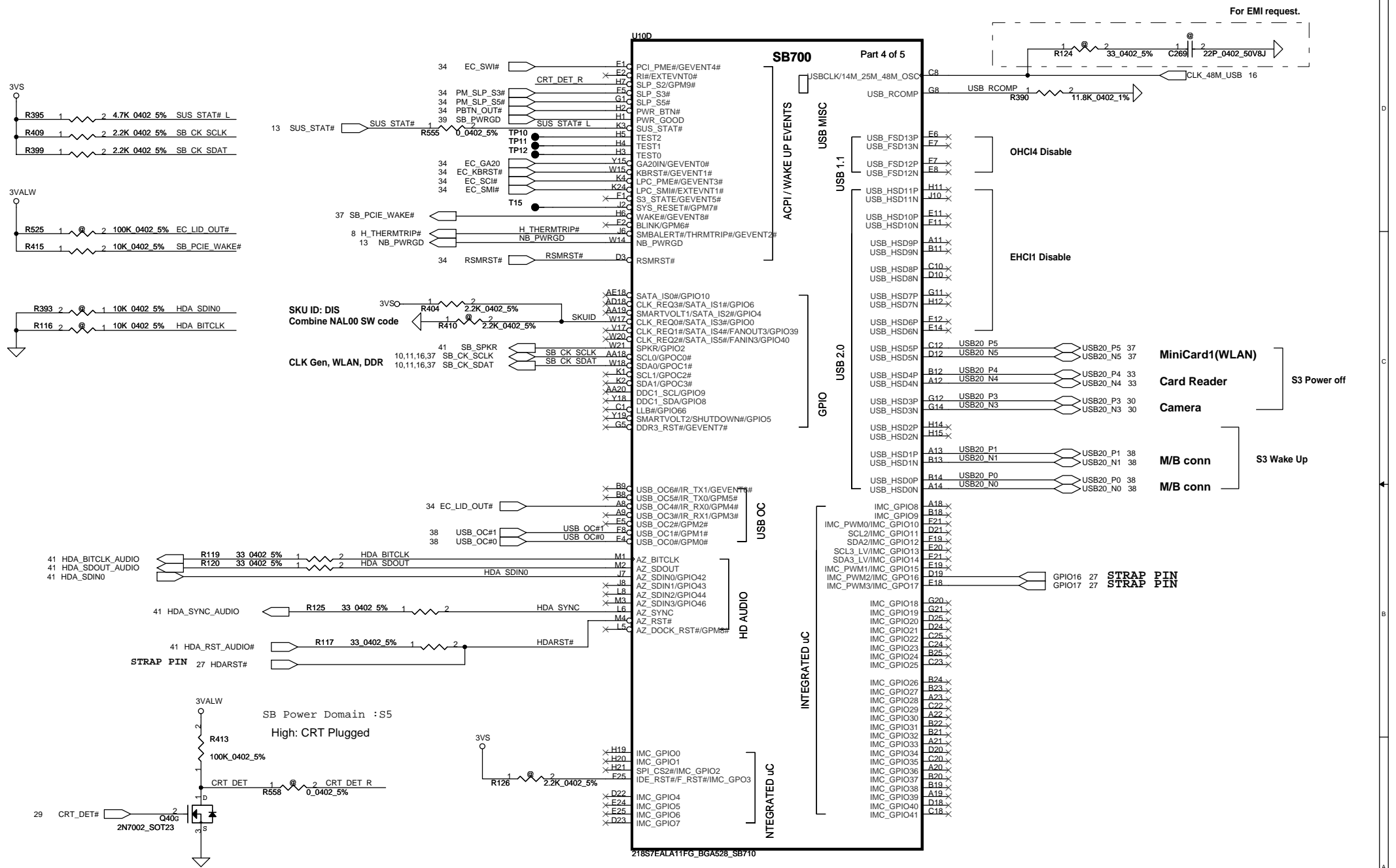
GPIO_28_TDO GPIO21_BB_EN

STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM ID 3,2,1,0
VRAM_ID[3:0]	DVPPDATA (3,2,1,0)	M92 S2-XT		512MB(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
				512MB(x4)	ATI 64Mx16 1.8V	SA00003LT10	0 0 1 0
				512MB(x4)	Samsung 64Mx16 1.8V (E-die)	SA000031O10	0 1 0 0

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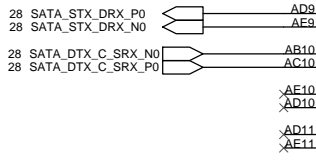
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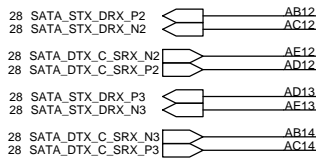
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Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller

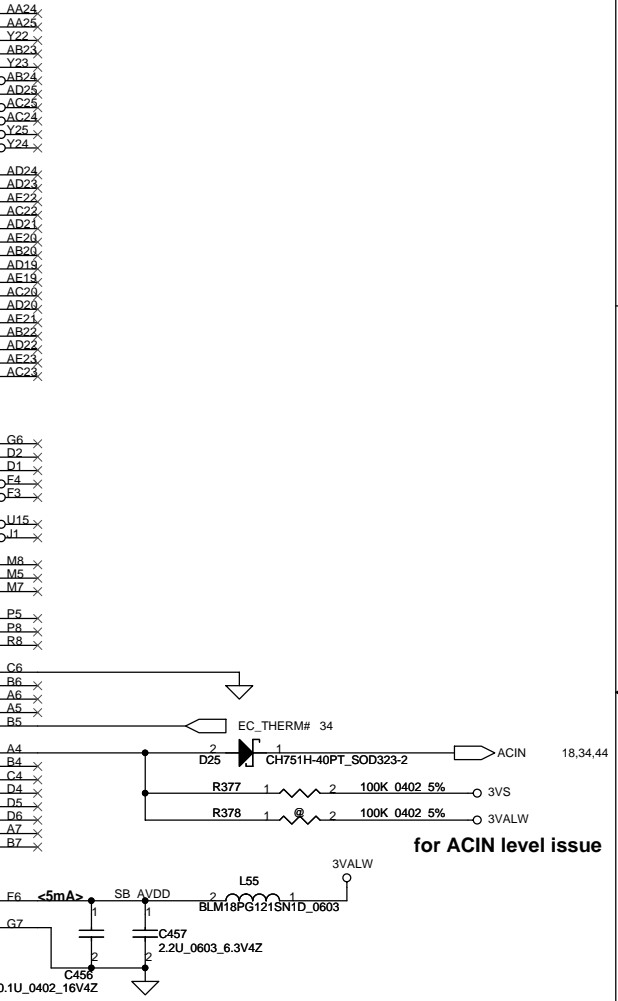
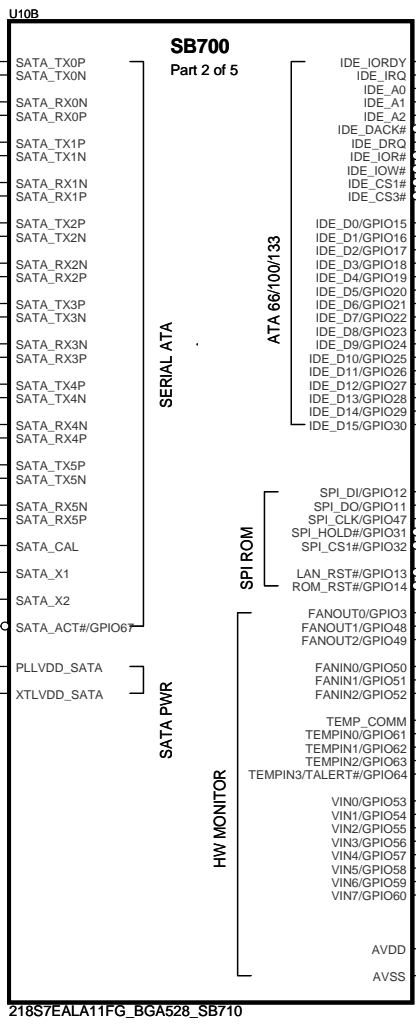
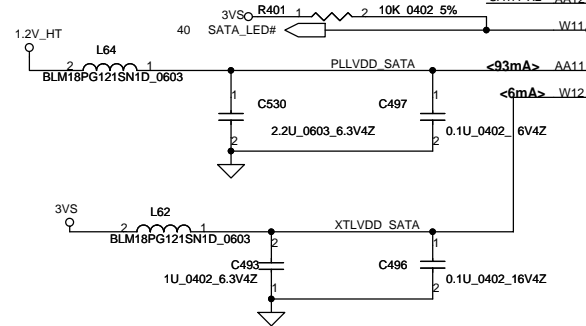
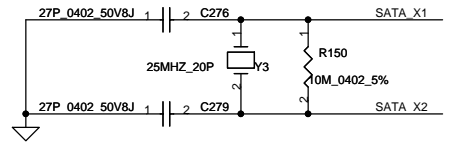
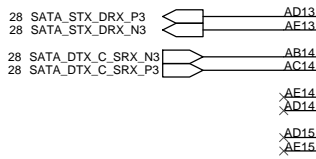
Main HDD



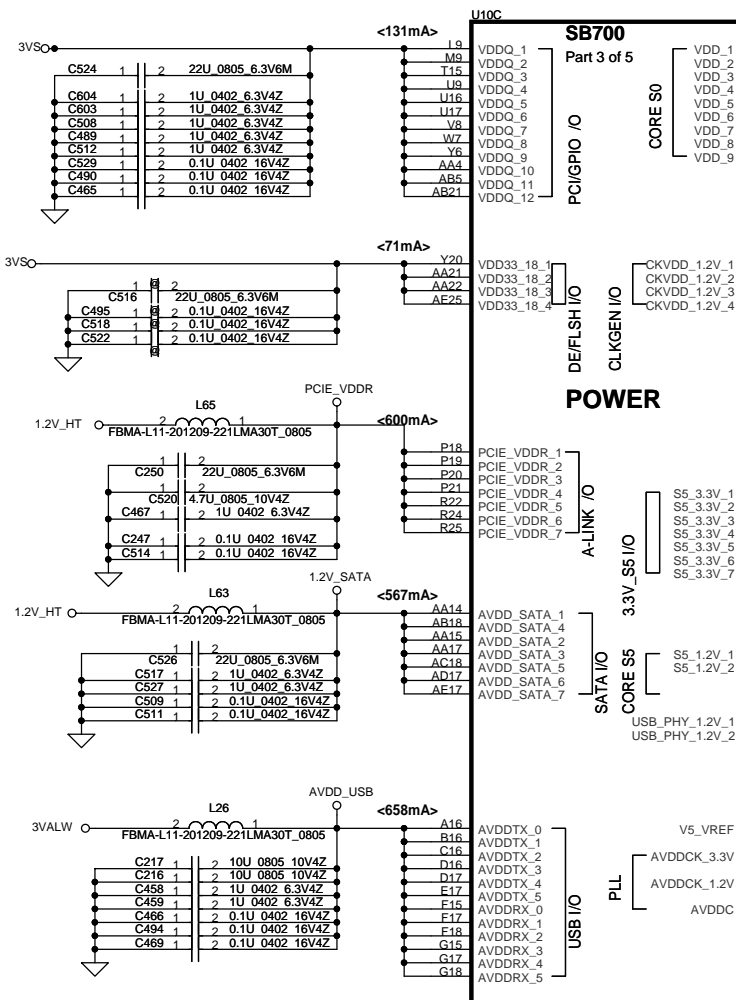
Main ODD



2nd ODD

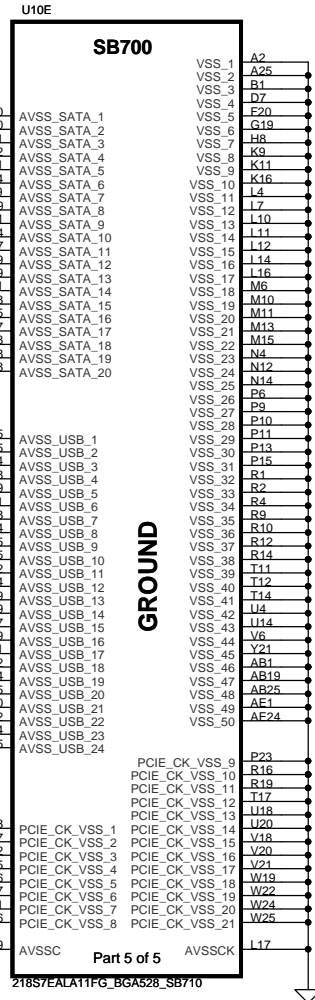
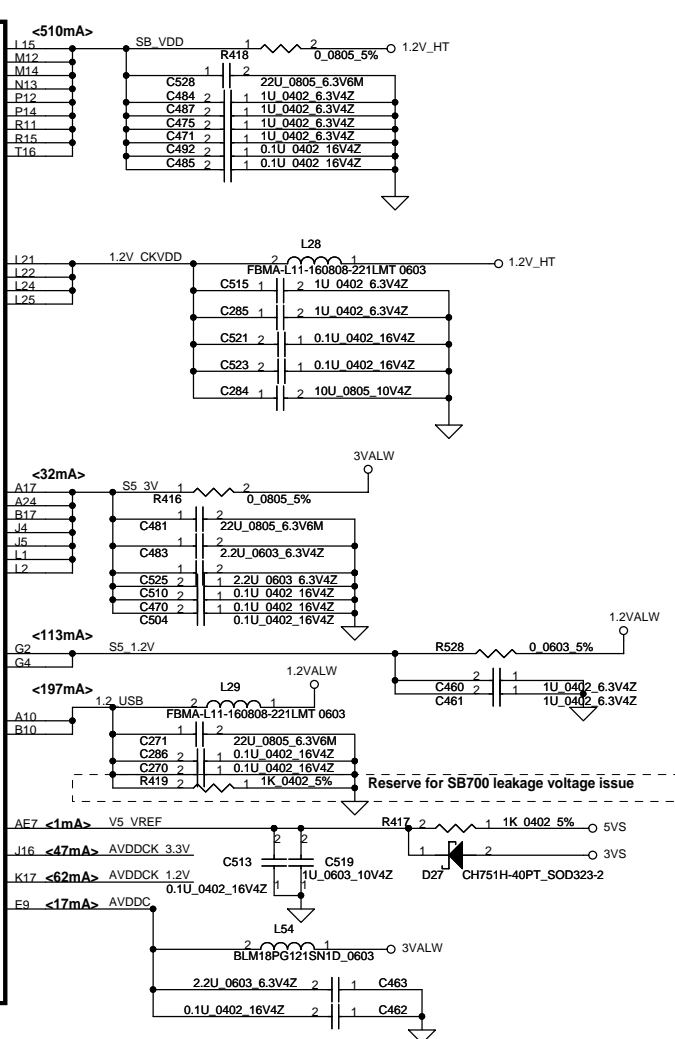
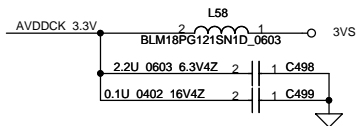
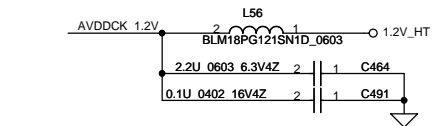


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218S7EAL11FG_BGA528_SB710

SB710 Ver:A14 <SA000030740>



218S7EAL11FG_BGA528_SB710

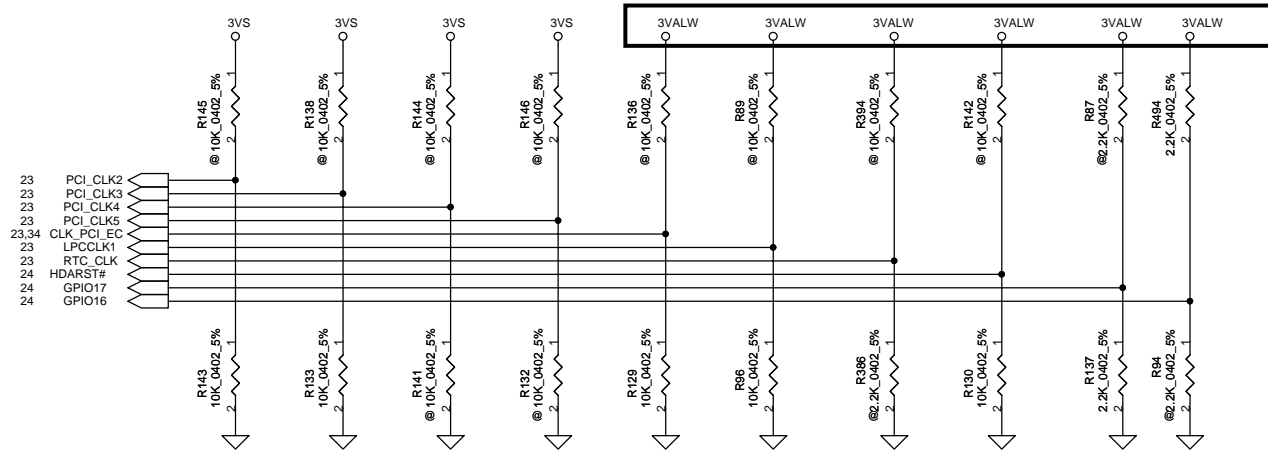
SB710 Ver:A14 <SA000030740>

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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

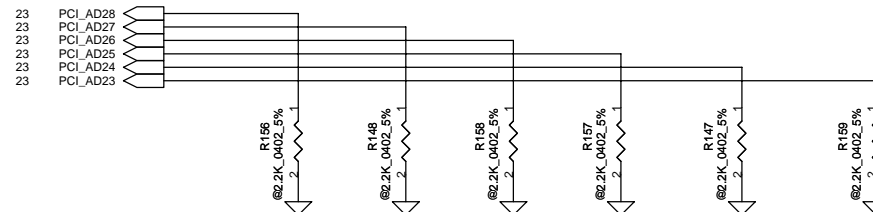
PULL	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
	HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM
LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L_NC) L,L = FWH ROM	



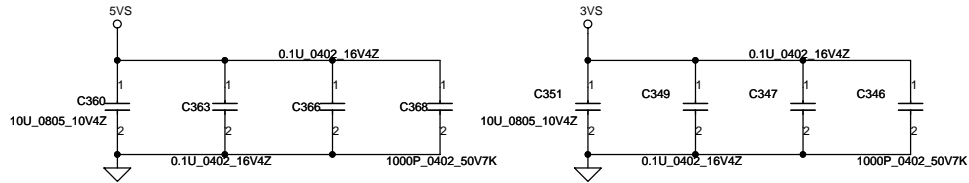
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

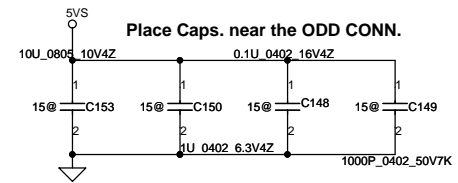
	PCI AD28	PCI AD27	PCI AD26	PCI AD25	PCI AD24	PCI AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



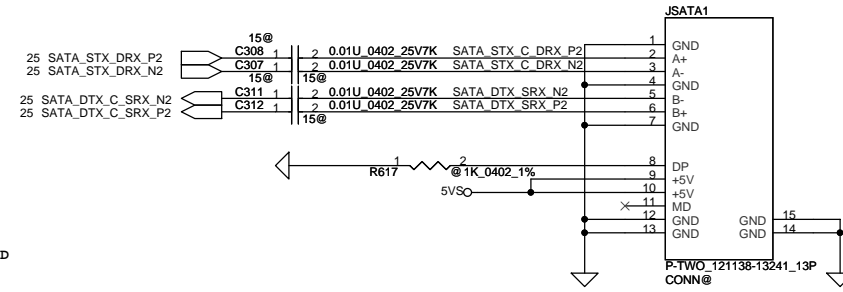
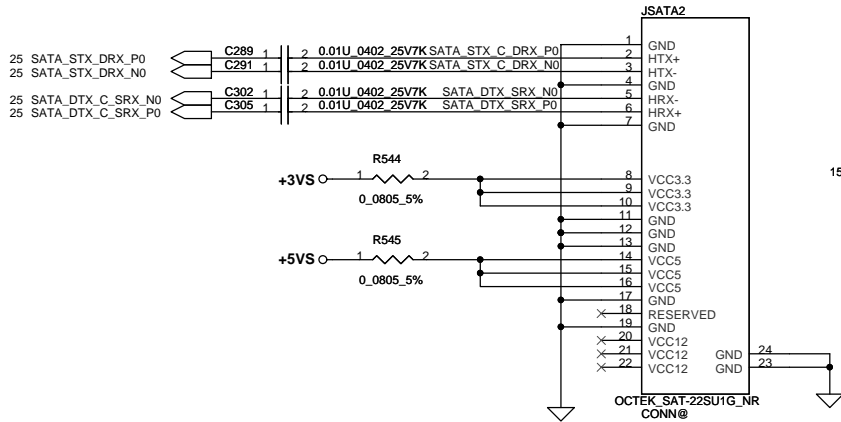
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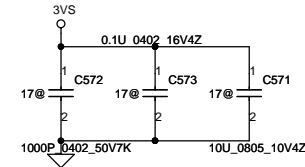
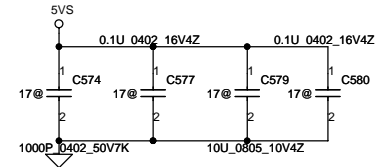
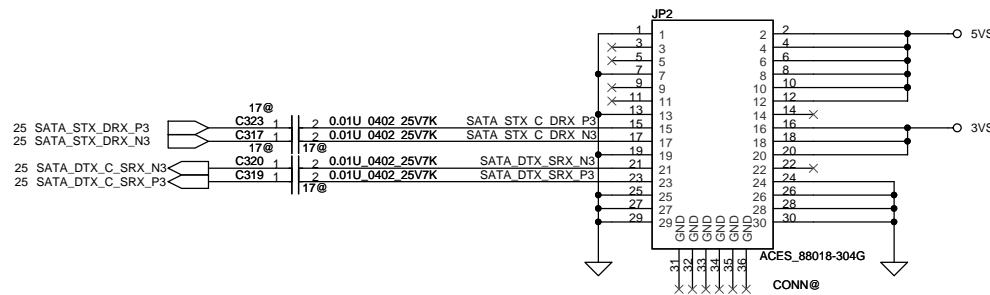
SATA HDD CONN



SATA ODD CONN

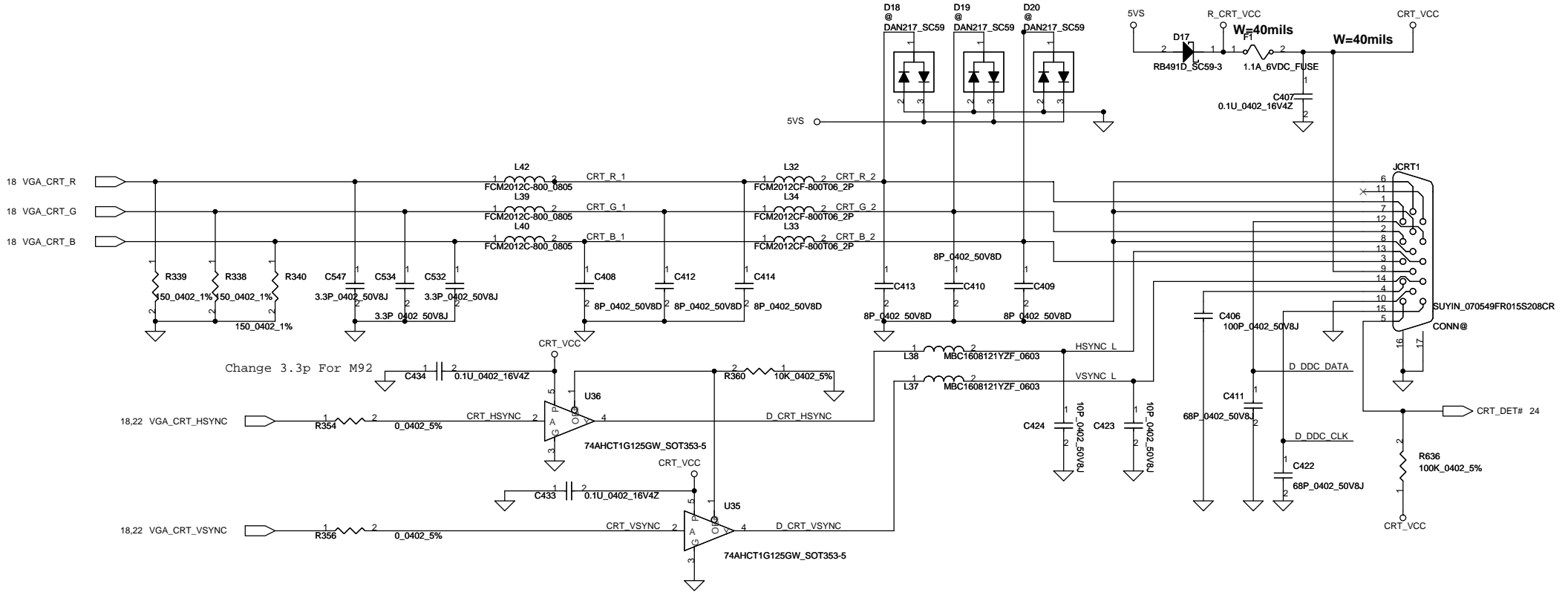


Second ODD



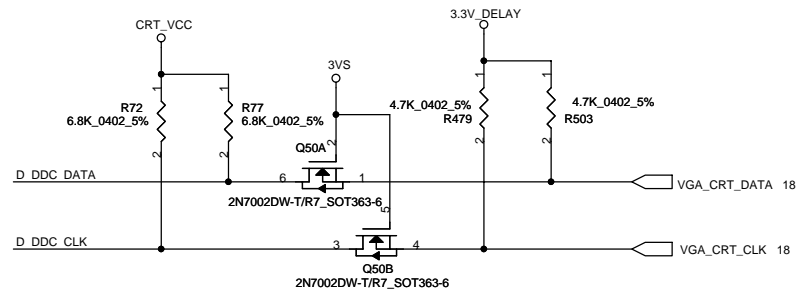
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CRT Connector



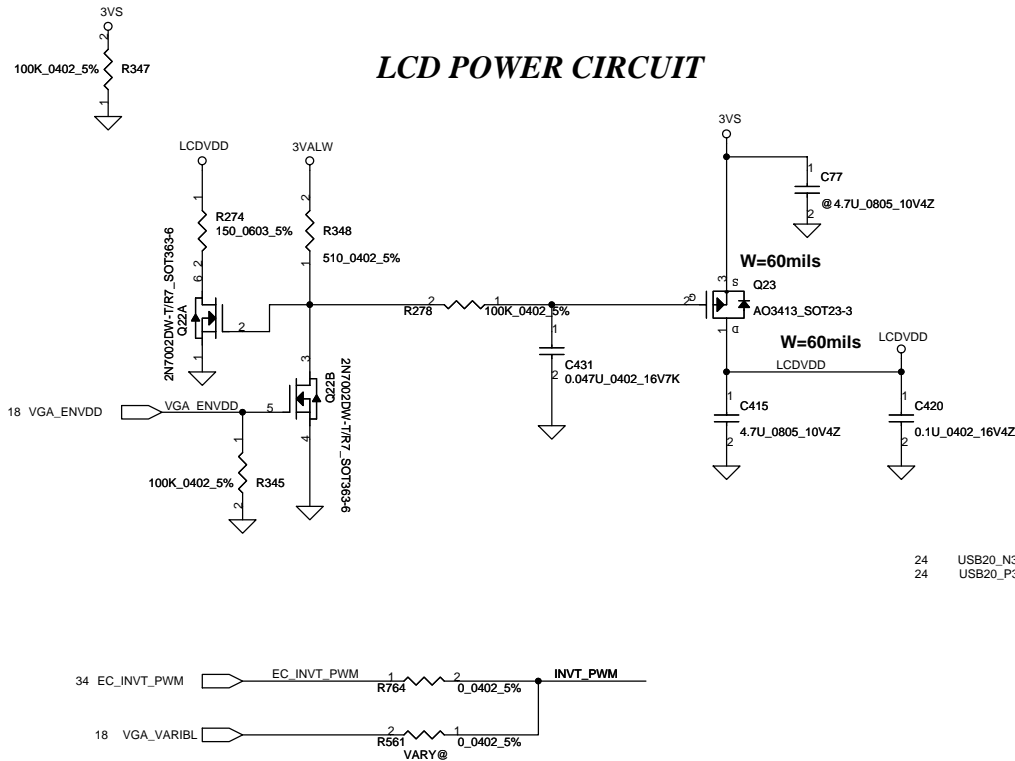
Change 3.3p For M92

Close to Conn side

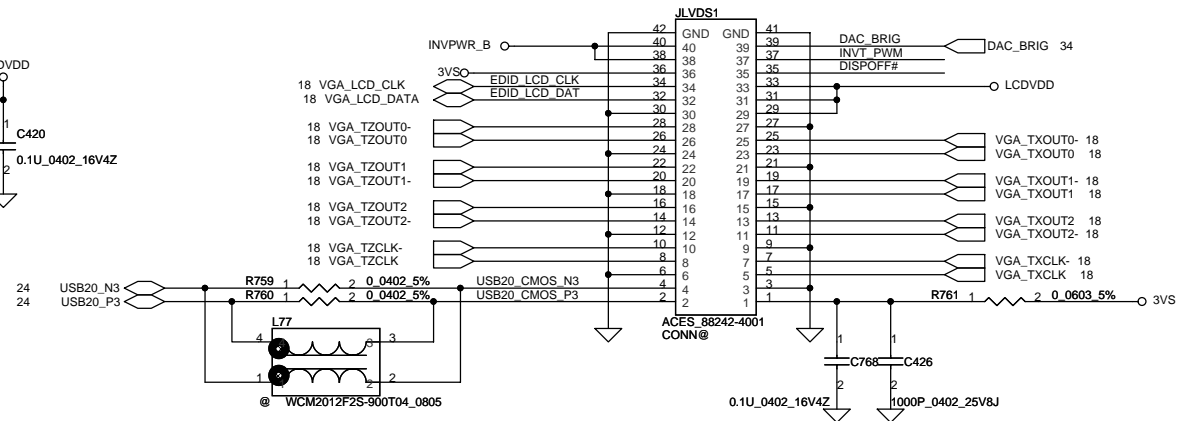


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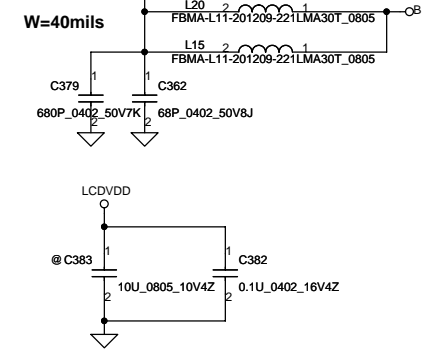
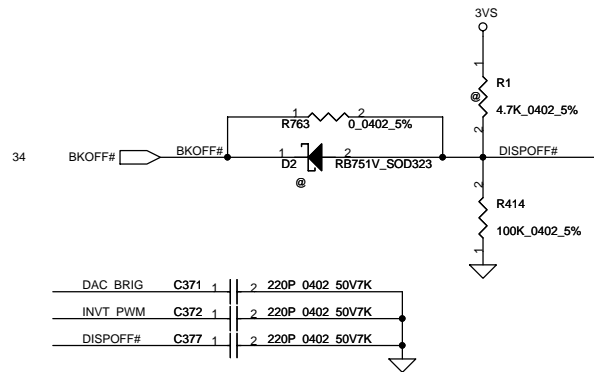
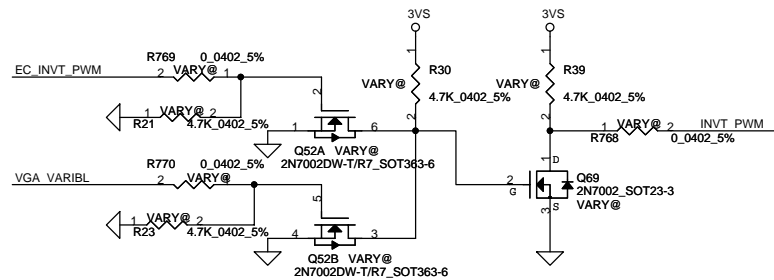
LCD POWER CIRCUIT



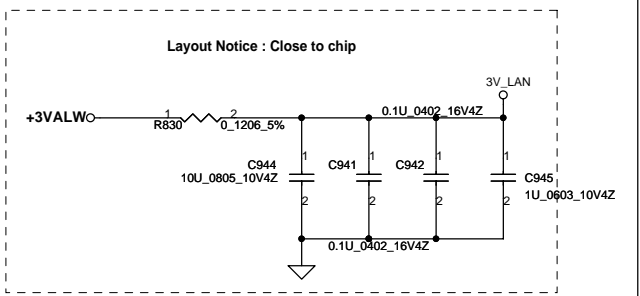
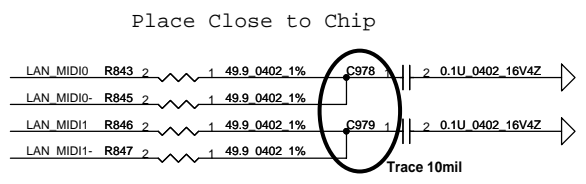
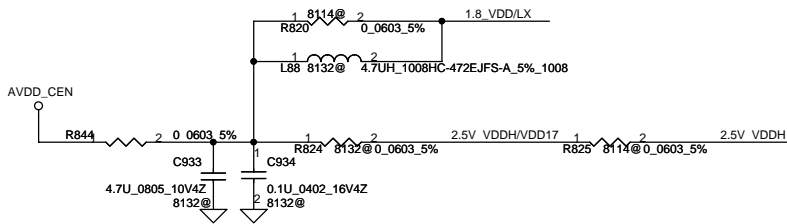
LCD/PANEL CONN.



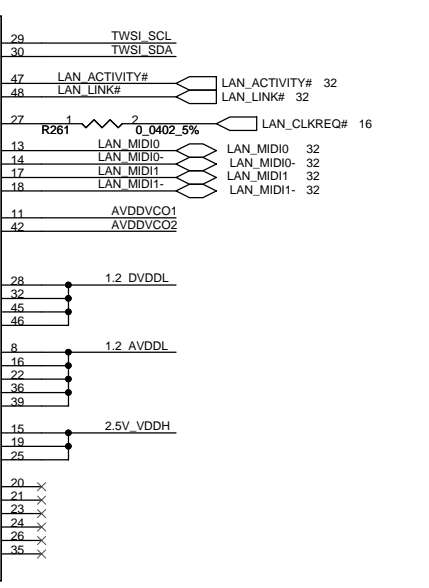
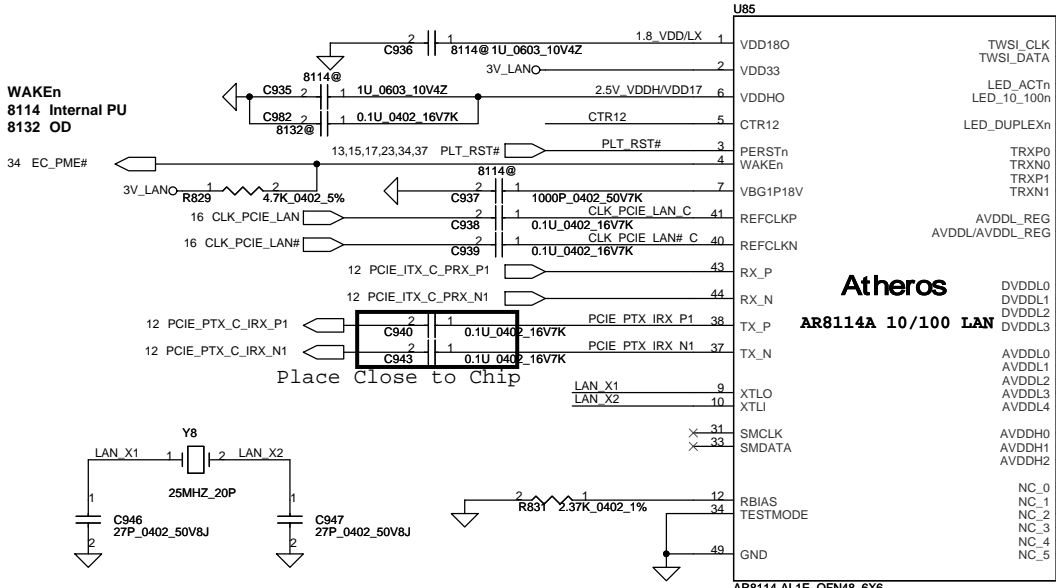
VARYBRIGHT FUNCTION



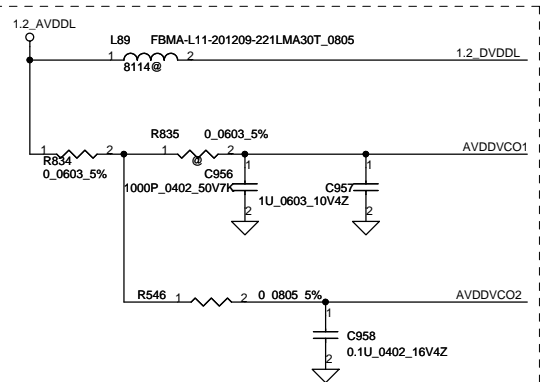
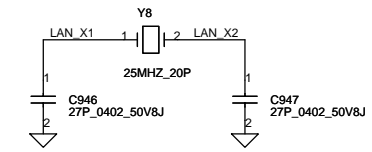
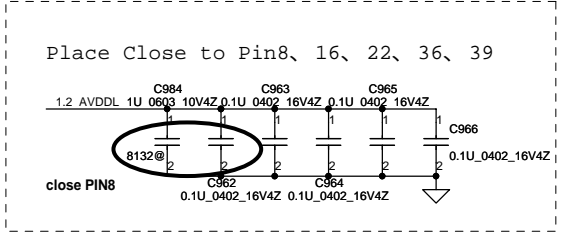
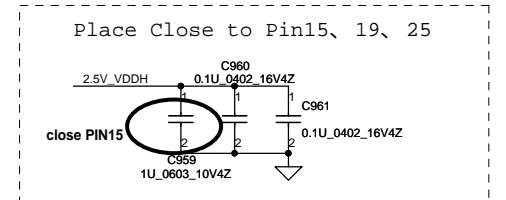
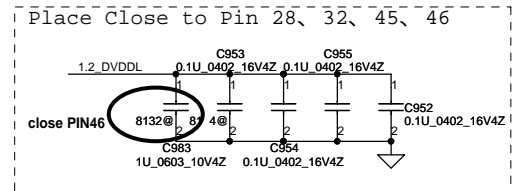
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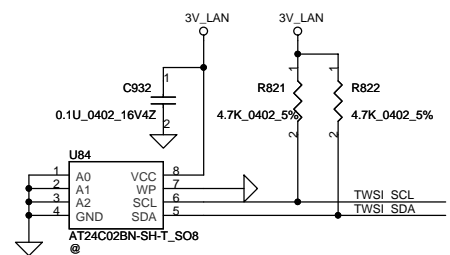
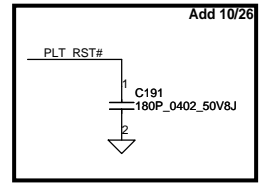
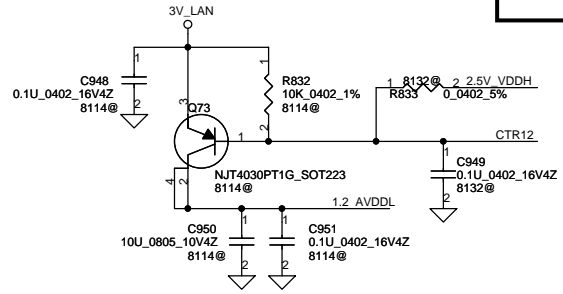
WAKEn
8114 Internal PU
8132 OD



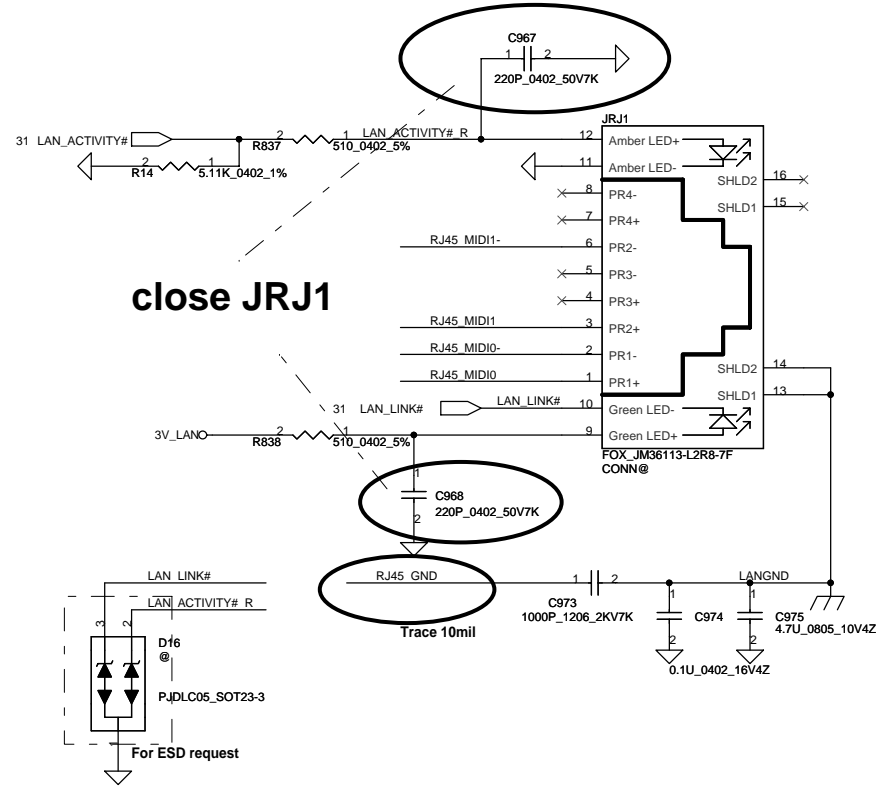
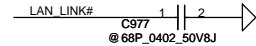
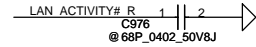
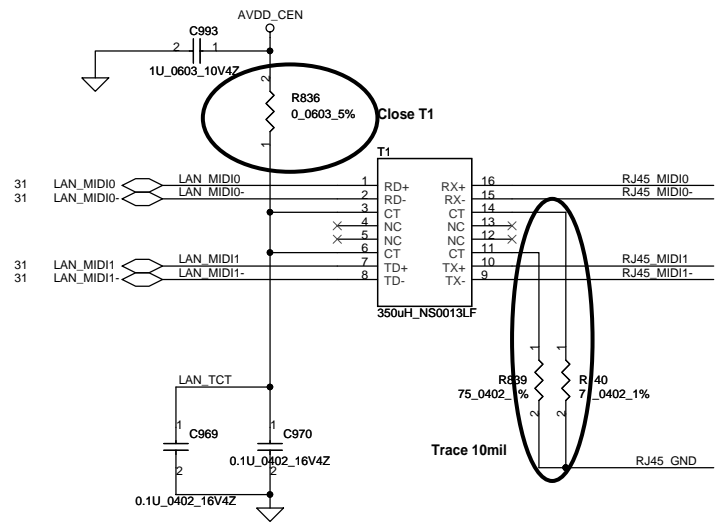
change to AR8132L-AL1E



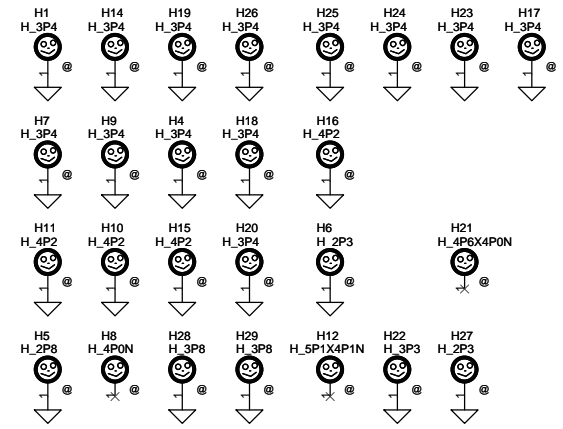
8114: R546 need change to bead



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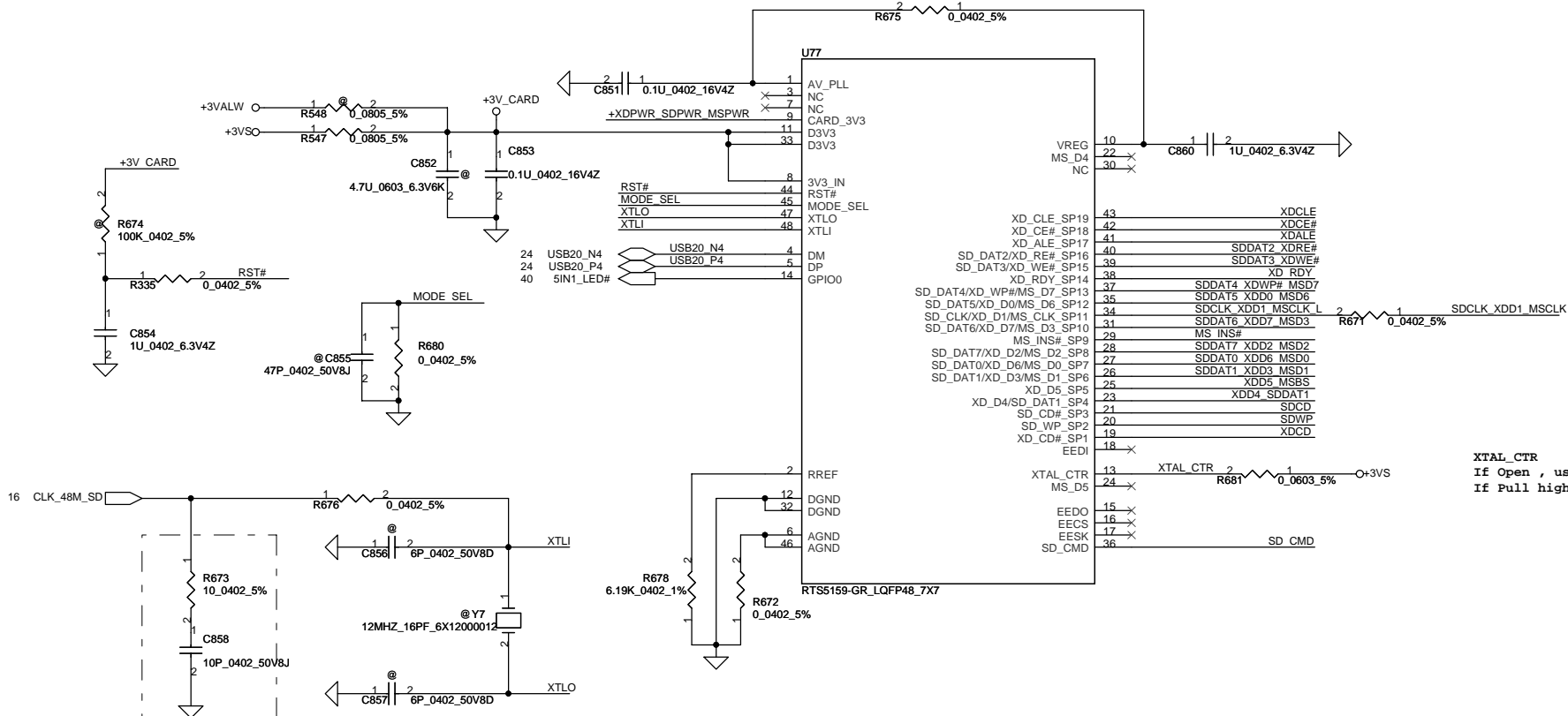
Screw Hole



PCB Federal Mark PAD

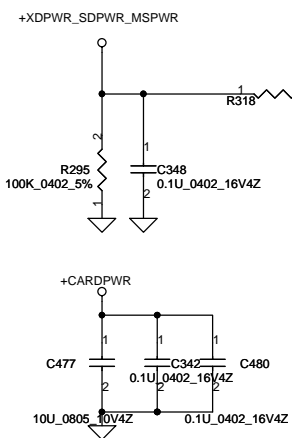


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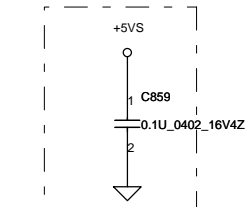


XTAL_CTR
 If Open , use 12MHz. crystal
 If Pull high , use CLKGEN 48MHz.

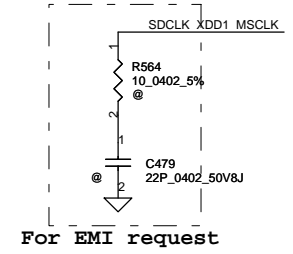
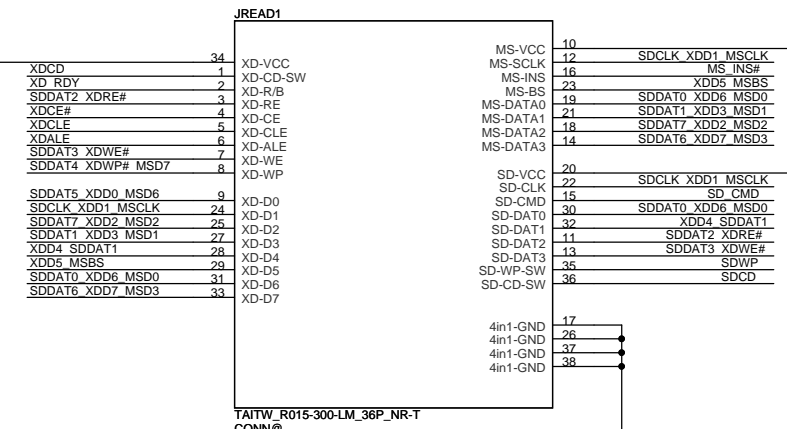
For EMI request



Close to CLK_SD_48M via

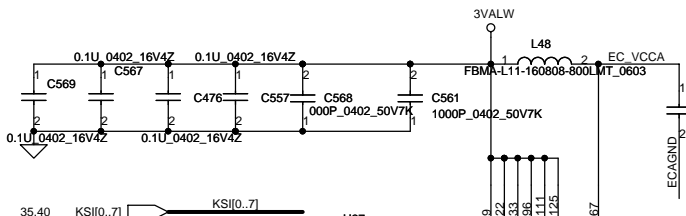
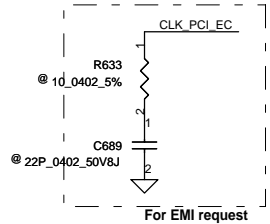


For EMI request

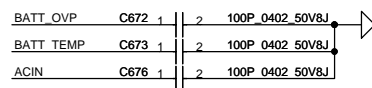


For EMI request

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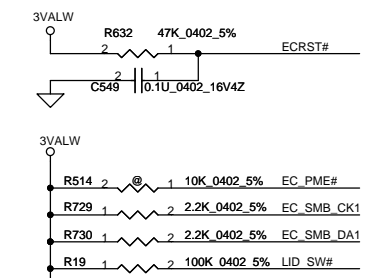
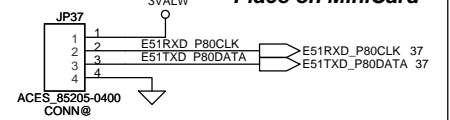


Please close to EC pin

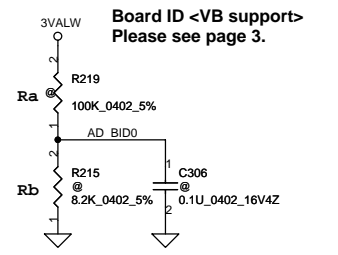
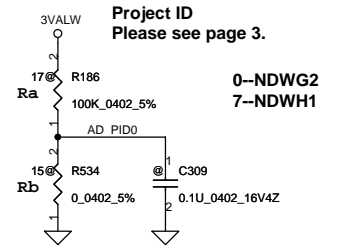
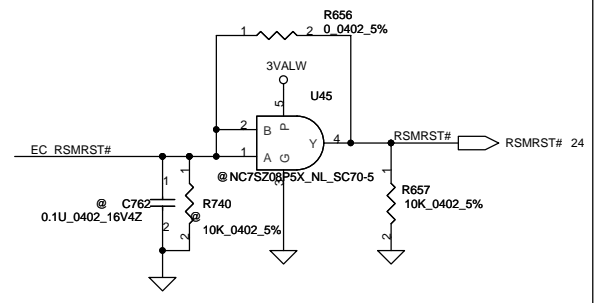
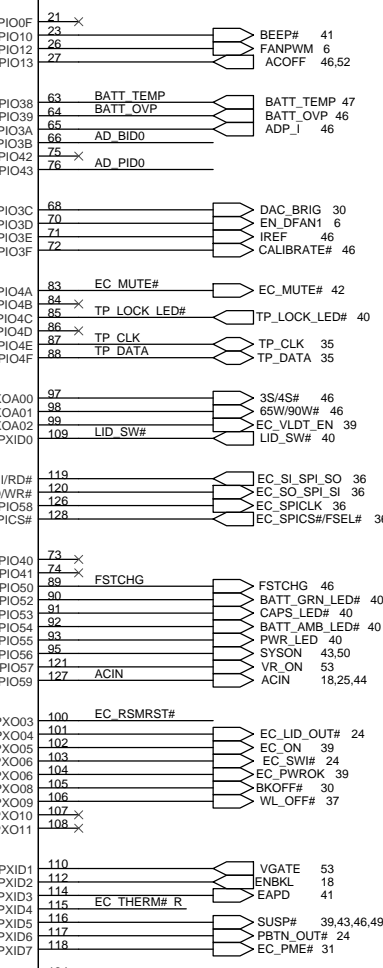
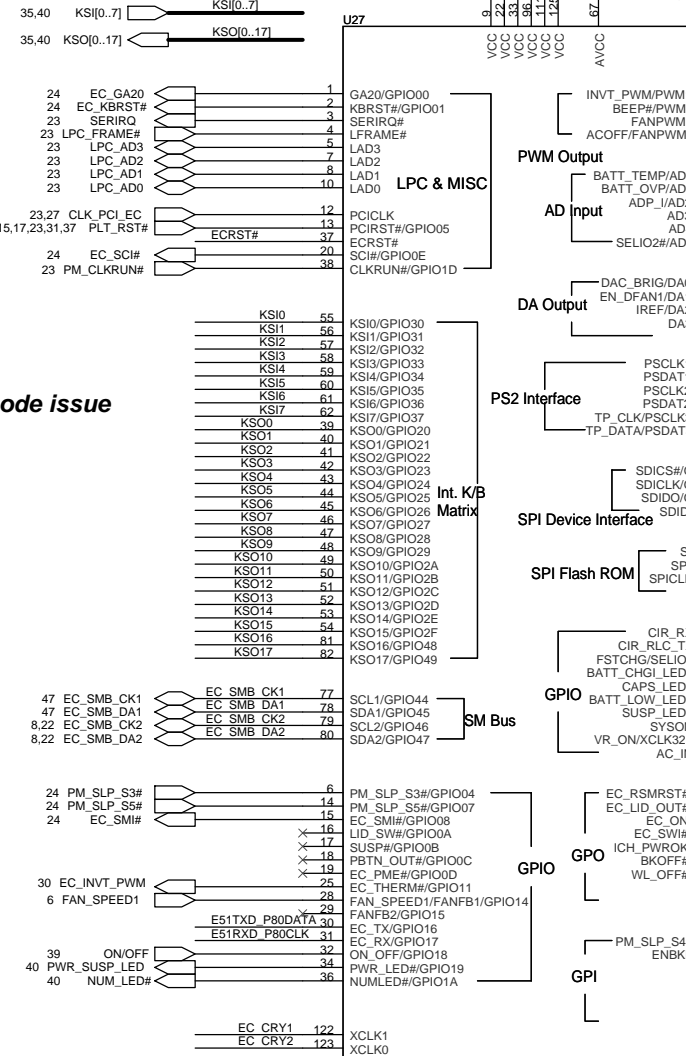
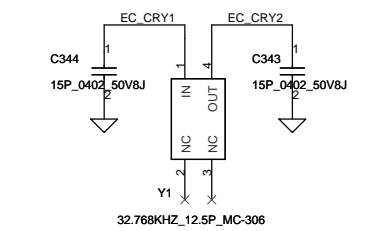
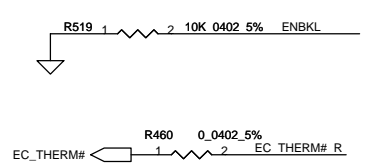
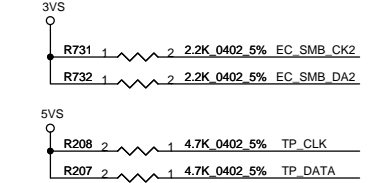


For EC Tools

Place on MiniCard



EC test-mode issue

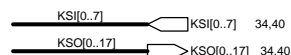
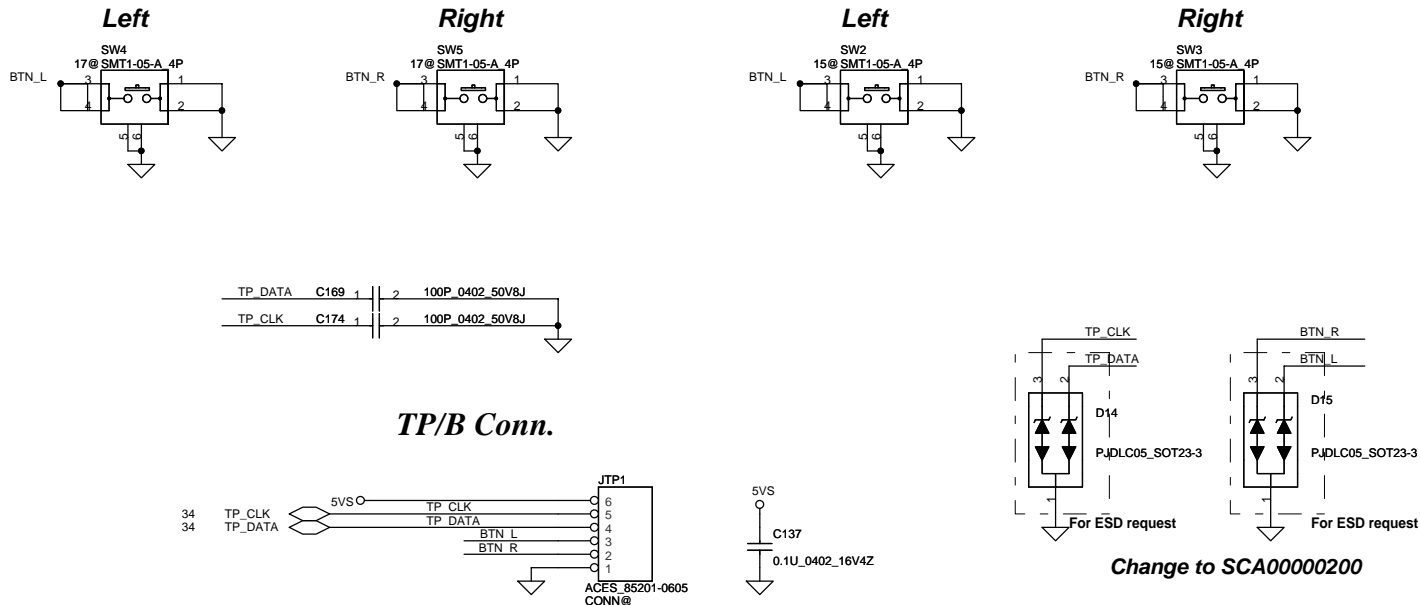


Chagne to D3 version

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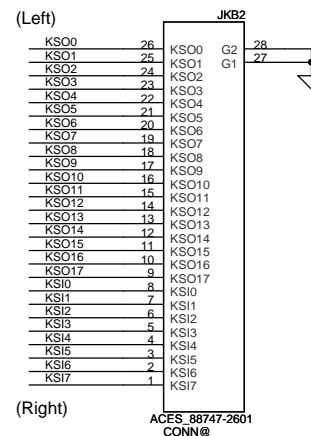
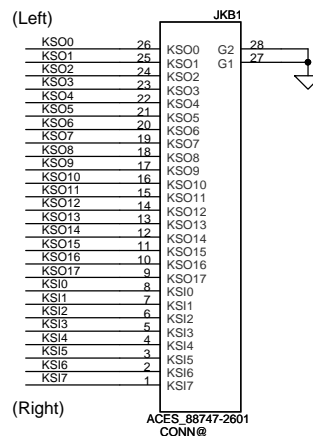
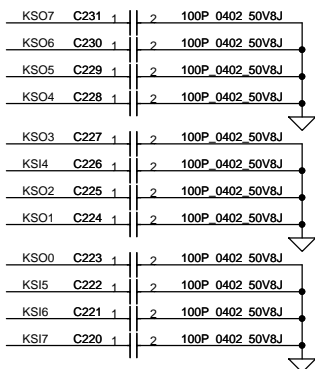
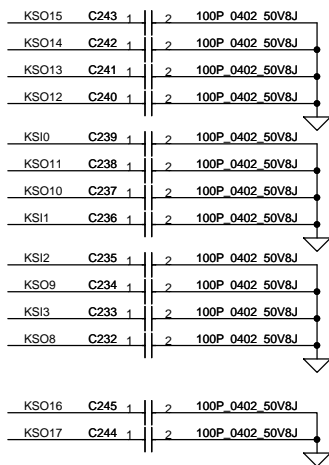
For 17"

For 15"



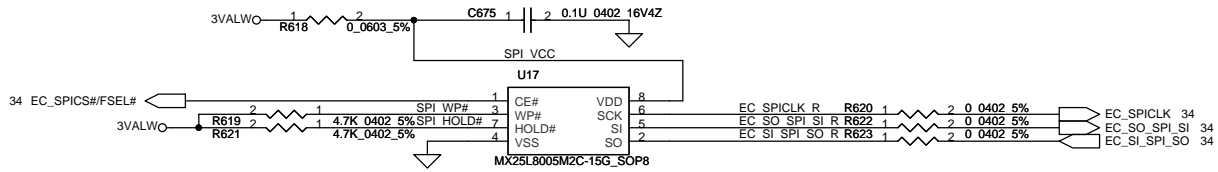
INT_KBD Conn.

KB1 for 15"
KB2 for 17"



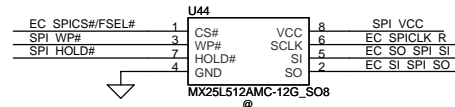
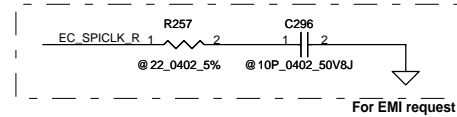
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SPI Flash ROM 16M*1



SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

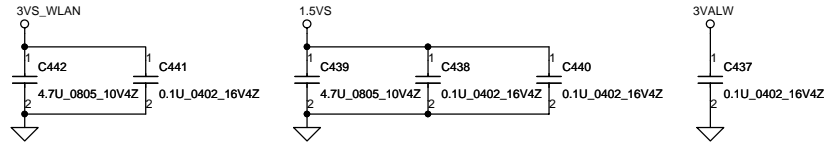
ONLY MXIC used in this project (66MHz)



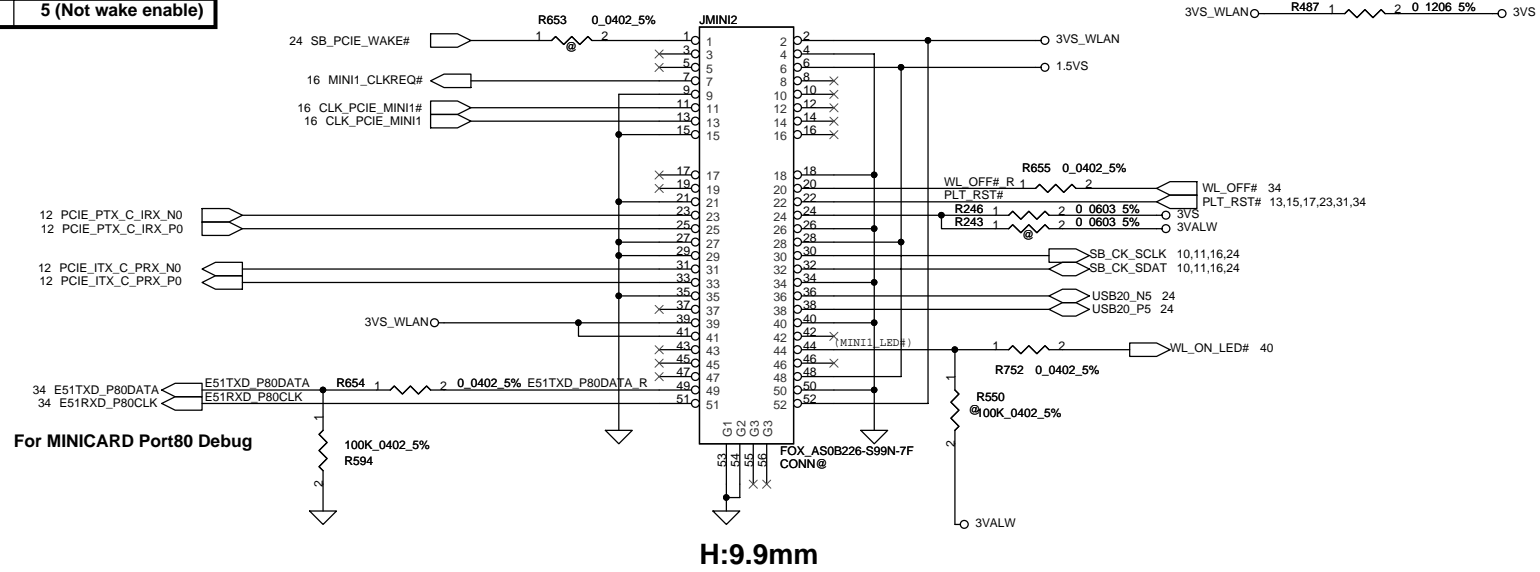
**Reserved for BIOS simulator.
 Footprint SO8
 SPI ROM Footprint 150mil**

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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

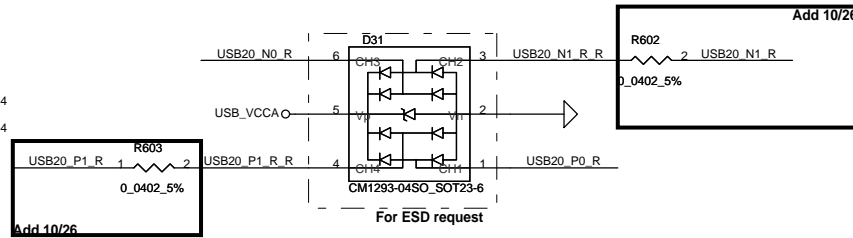
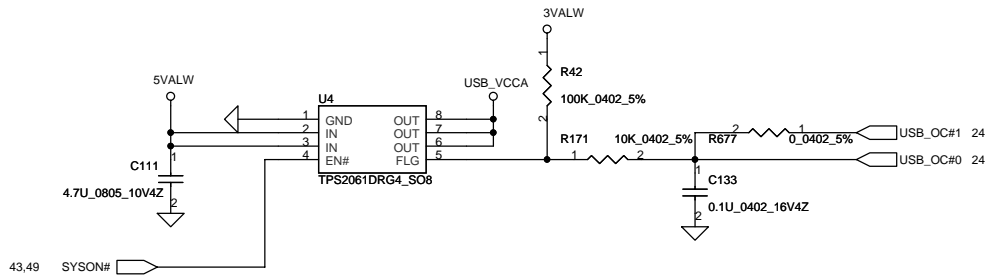
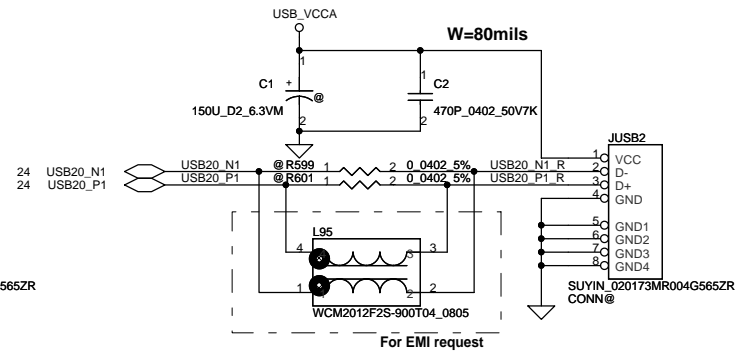
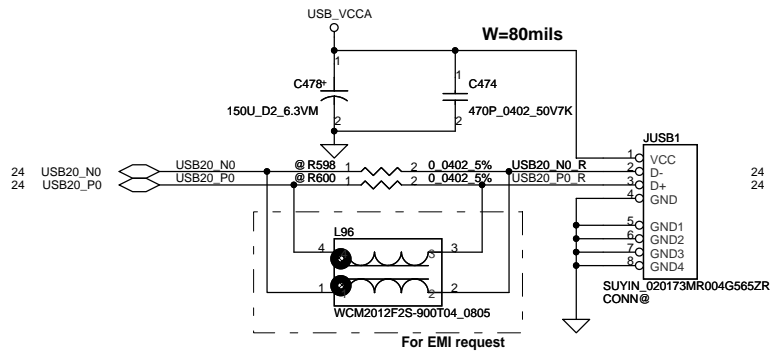


For Wireless LAN



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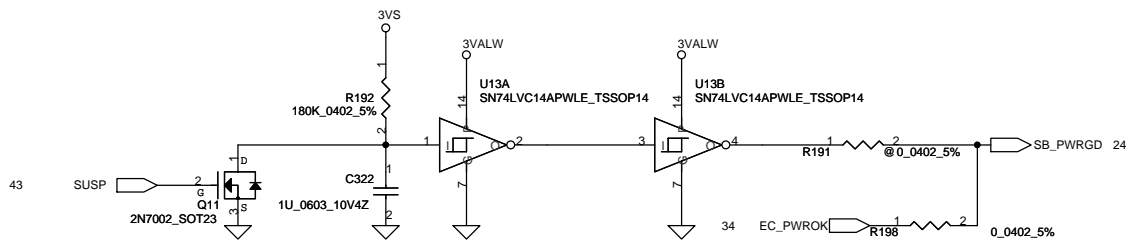
USB CONN. 1 & 2



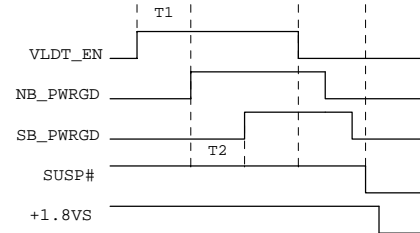
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Power ON Circuit

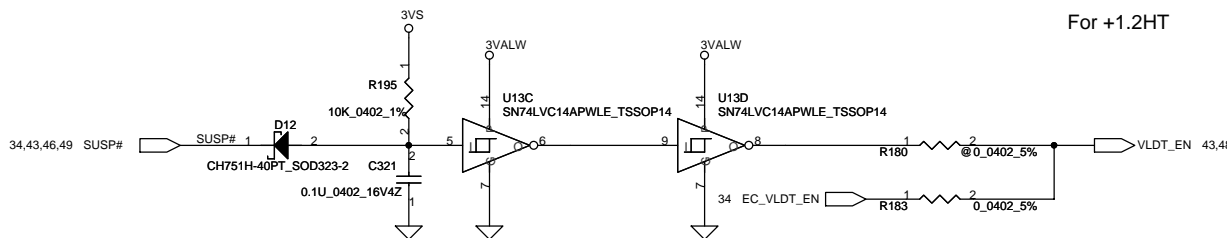
For South Bridge



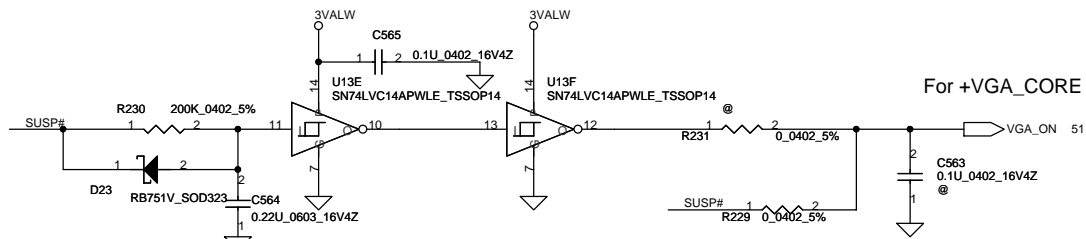
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



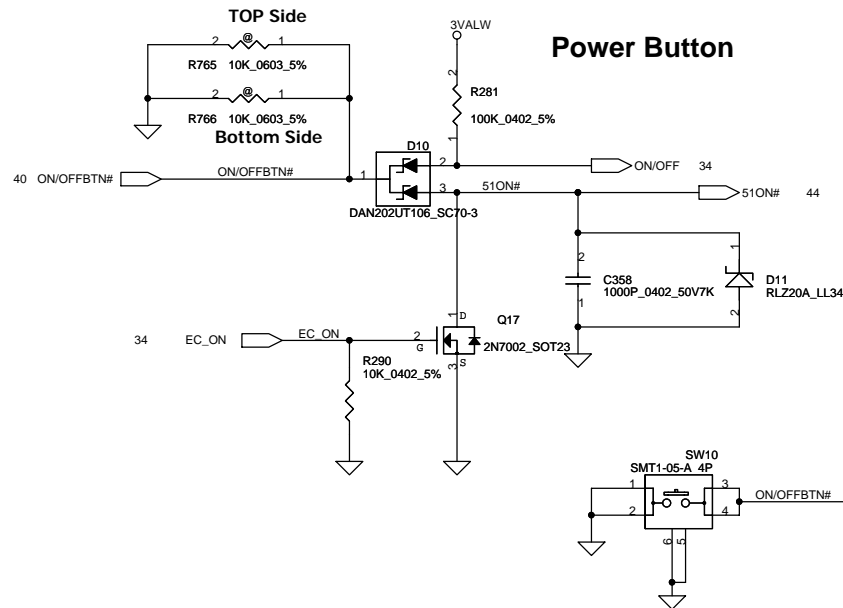
For +1.2HT



For +VGA_CORE

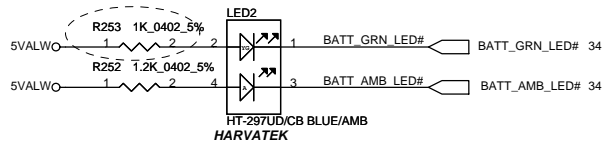
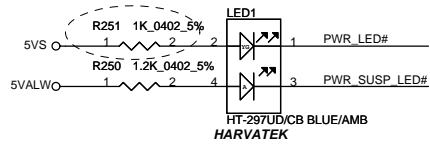
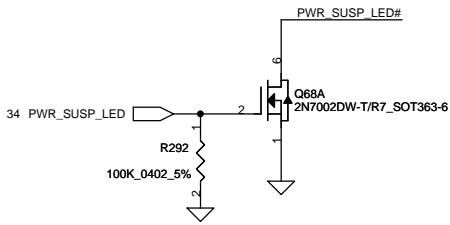
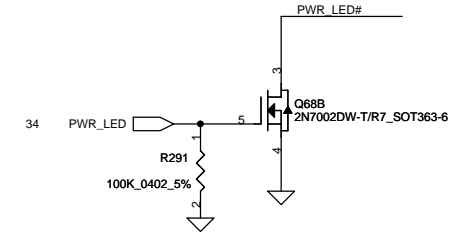


Power Button

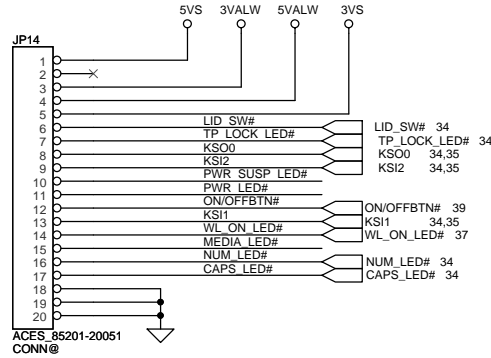


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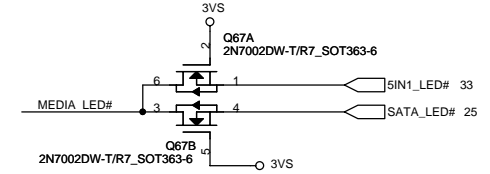
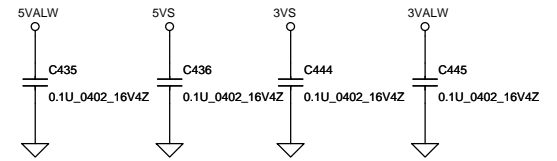
To PWR LED/B



BLUE/AMB LED

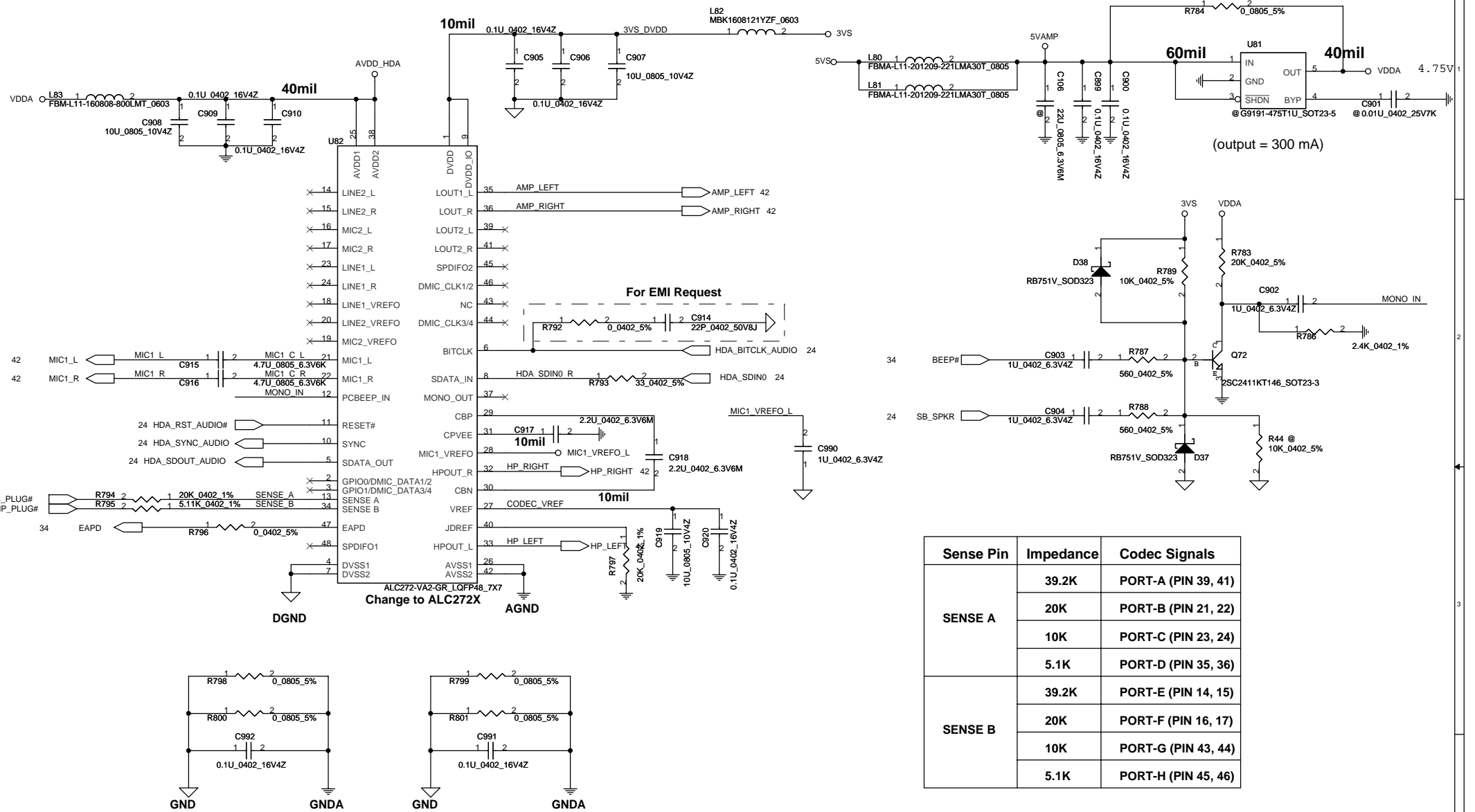


	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	

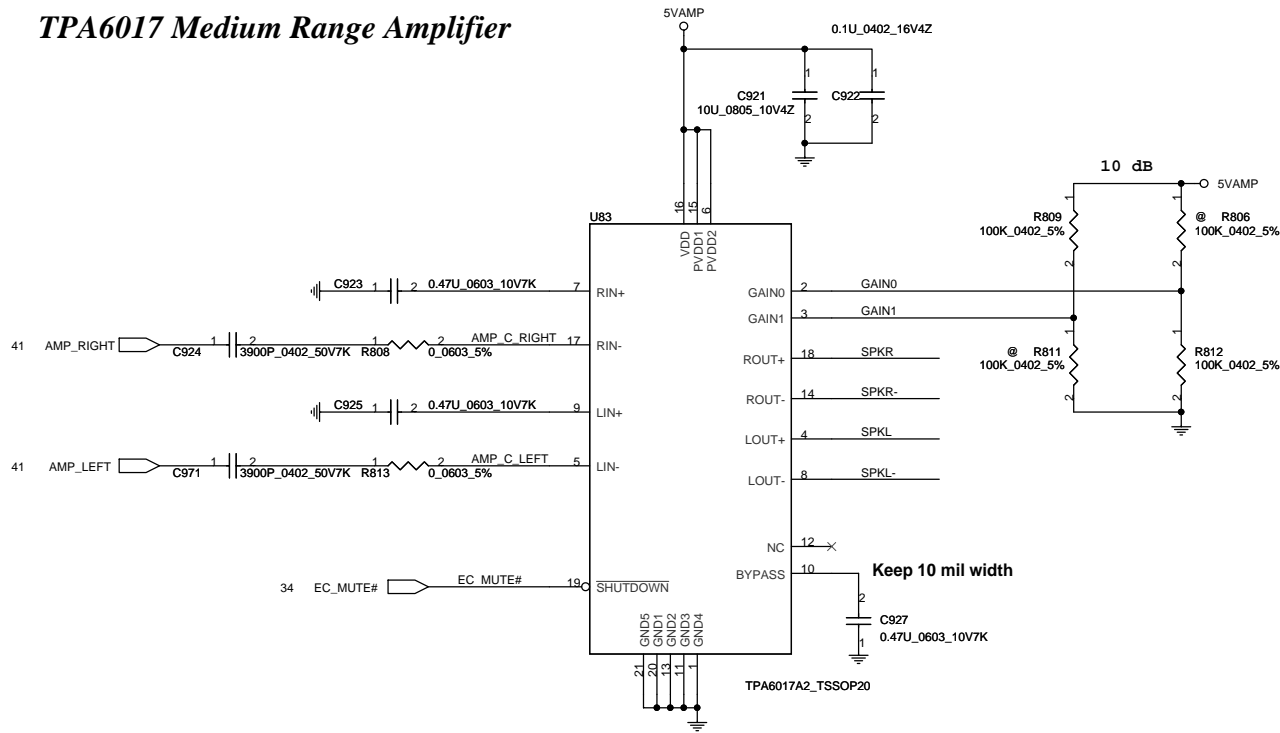


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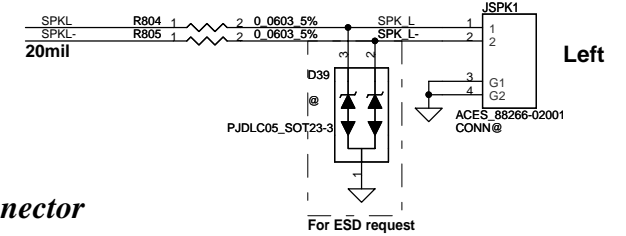
HD Audio Codec



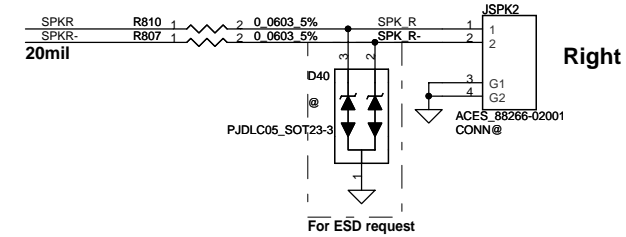
TPA6017 Medium Range Amplifier



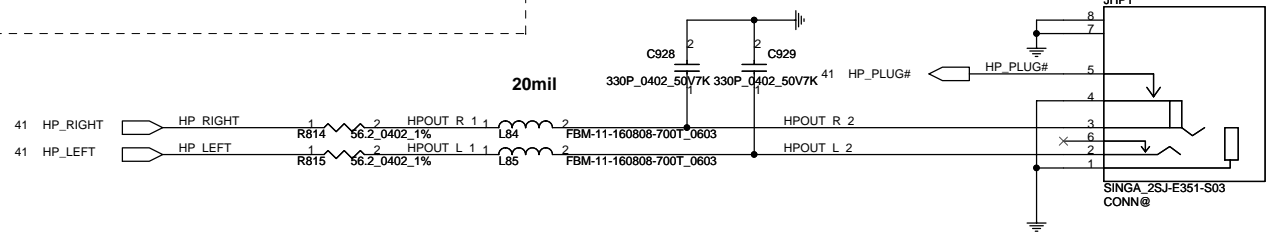
Left Connector



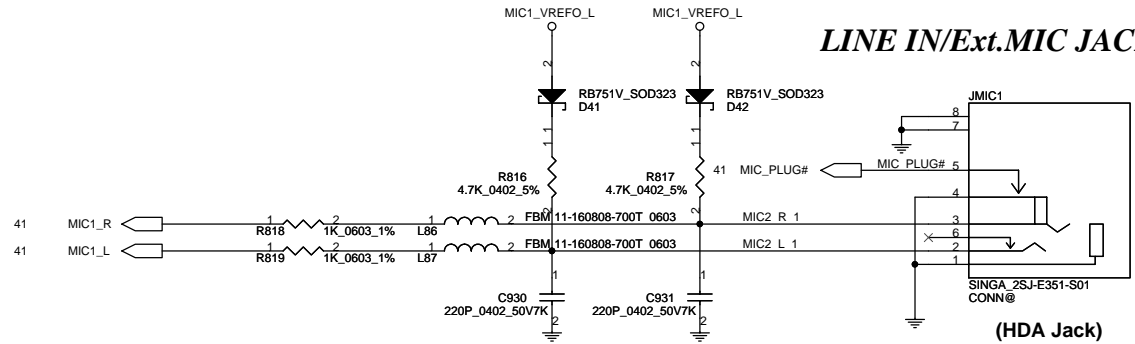
Right Connector



LINE Out/Headphone Out

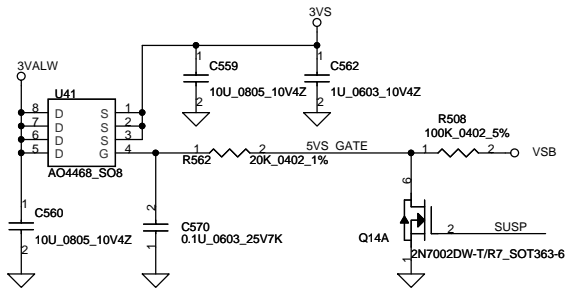


LINE IN/Ext.MIC JACK

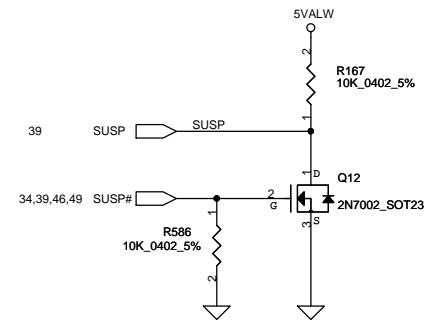
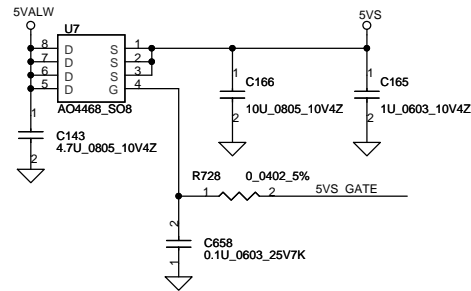


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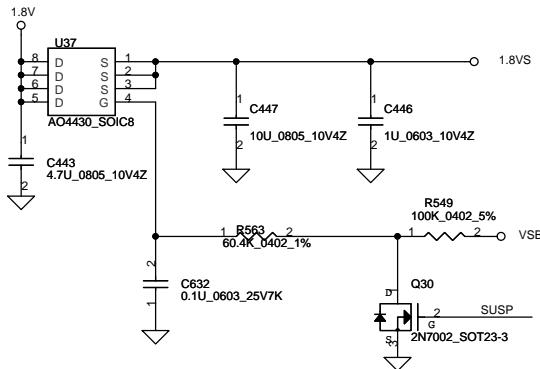
+3VALW TO +3VS



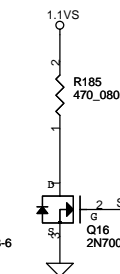
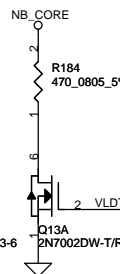
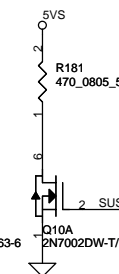
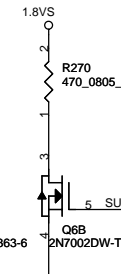
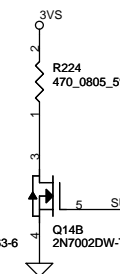
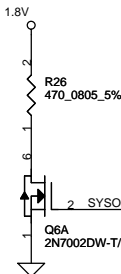
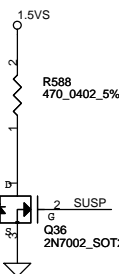
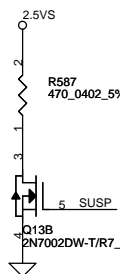
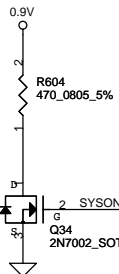
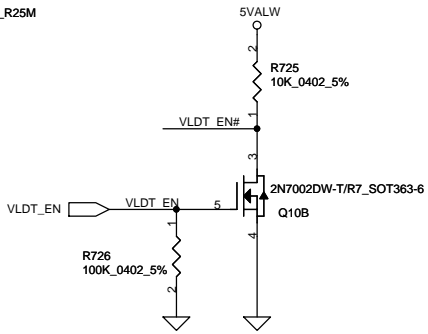
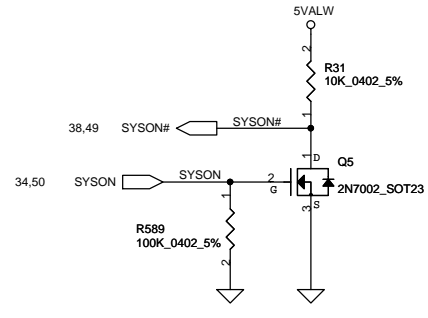
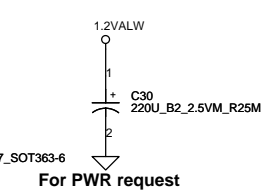
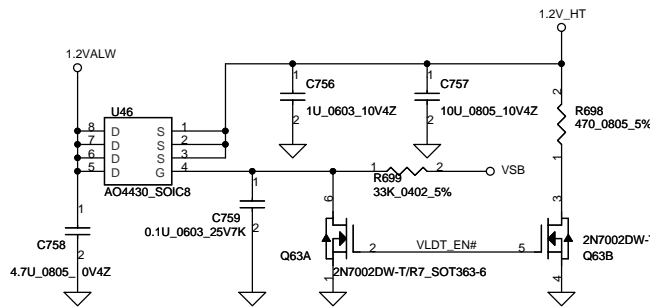
+5VALW TO +5VS



+1.8V TO +1.8VS



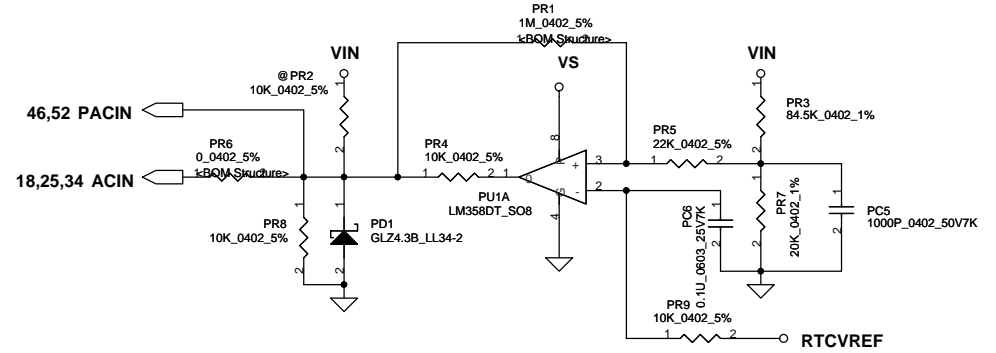
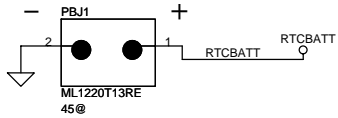
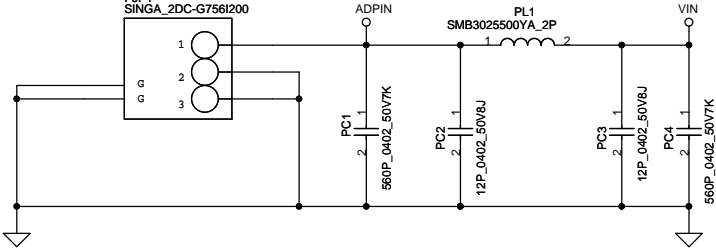
+1.2VALW TO +1.2V_HT



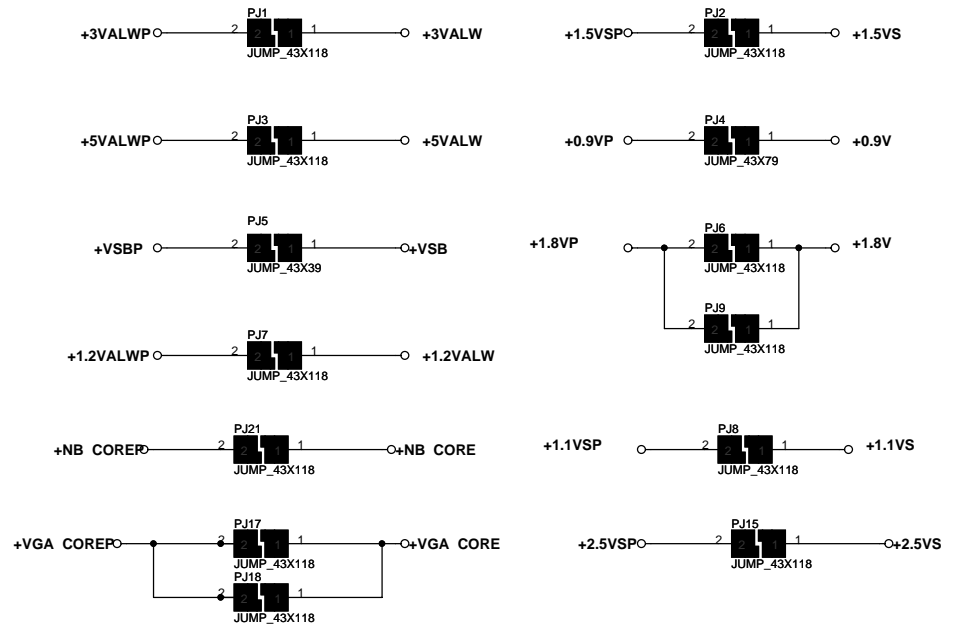
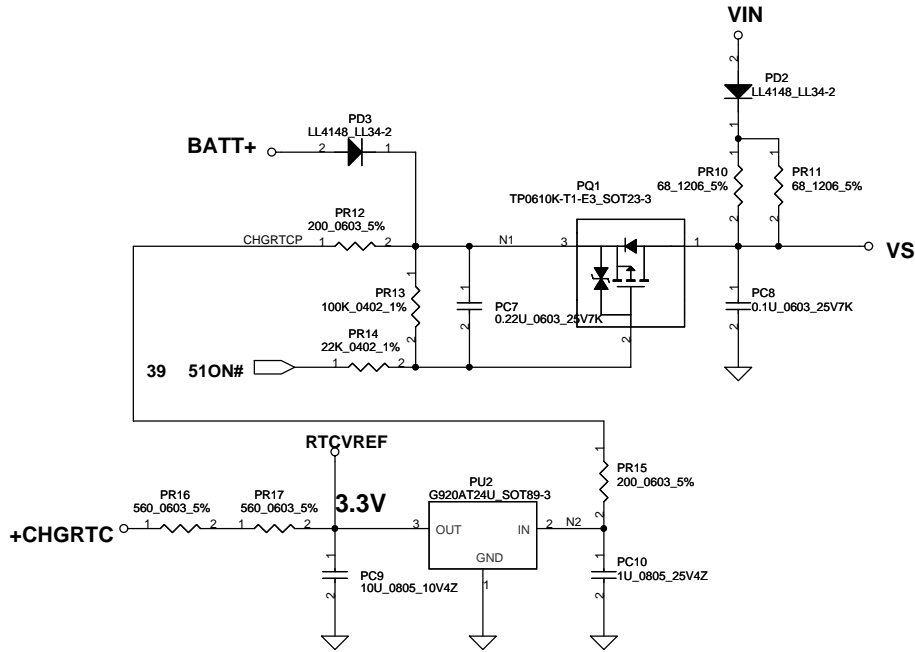
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DC231000500

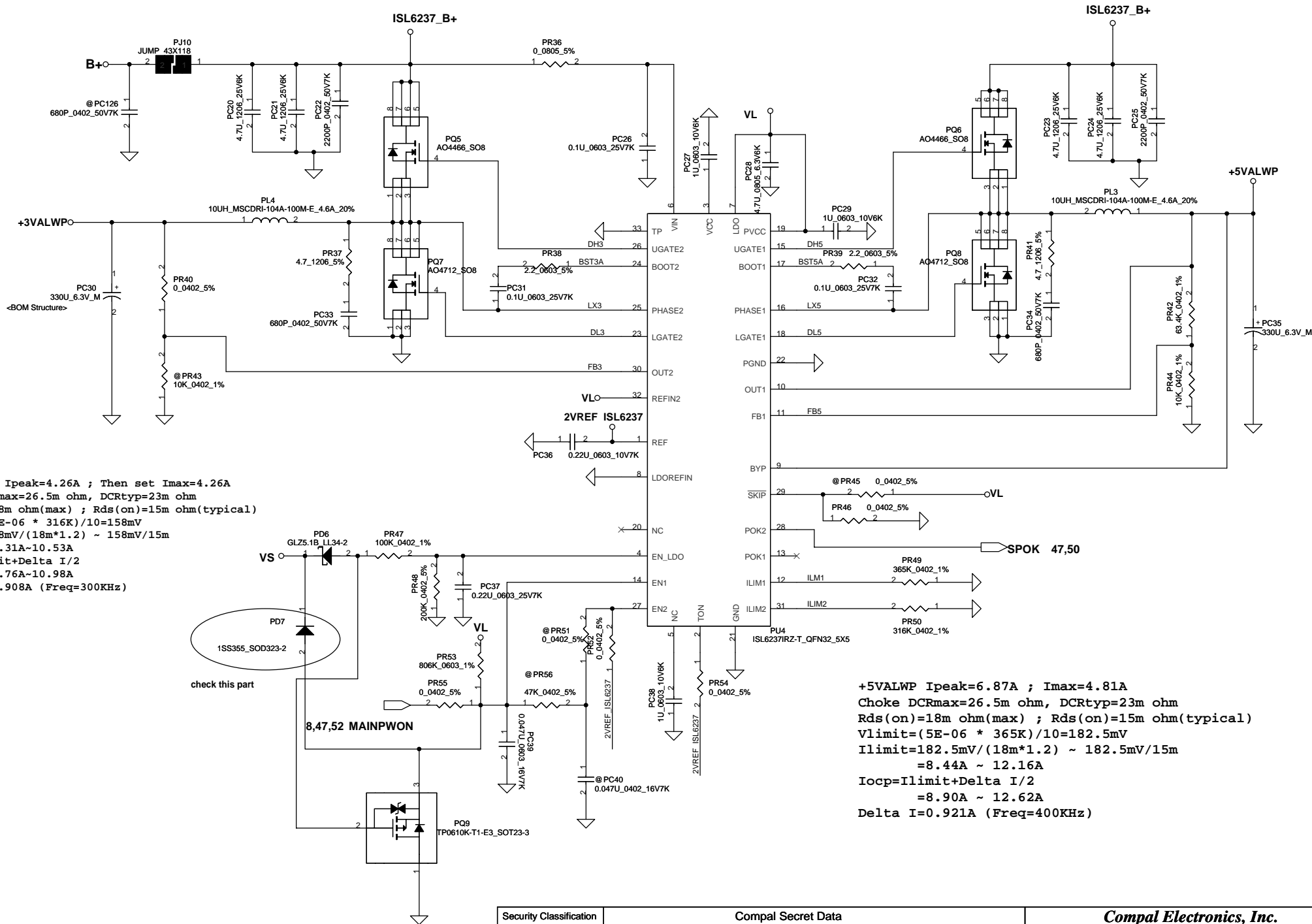
PCB Structure>
SINGA_2DC-G7561200



Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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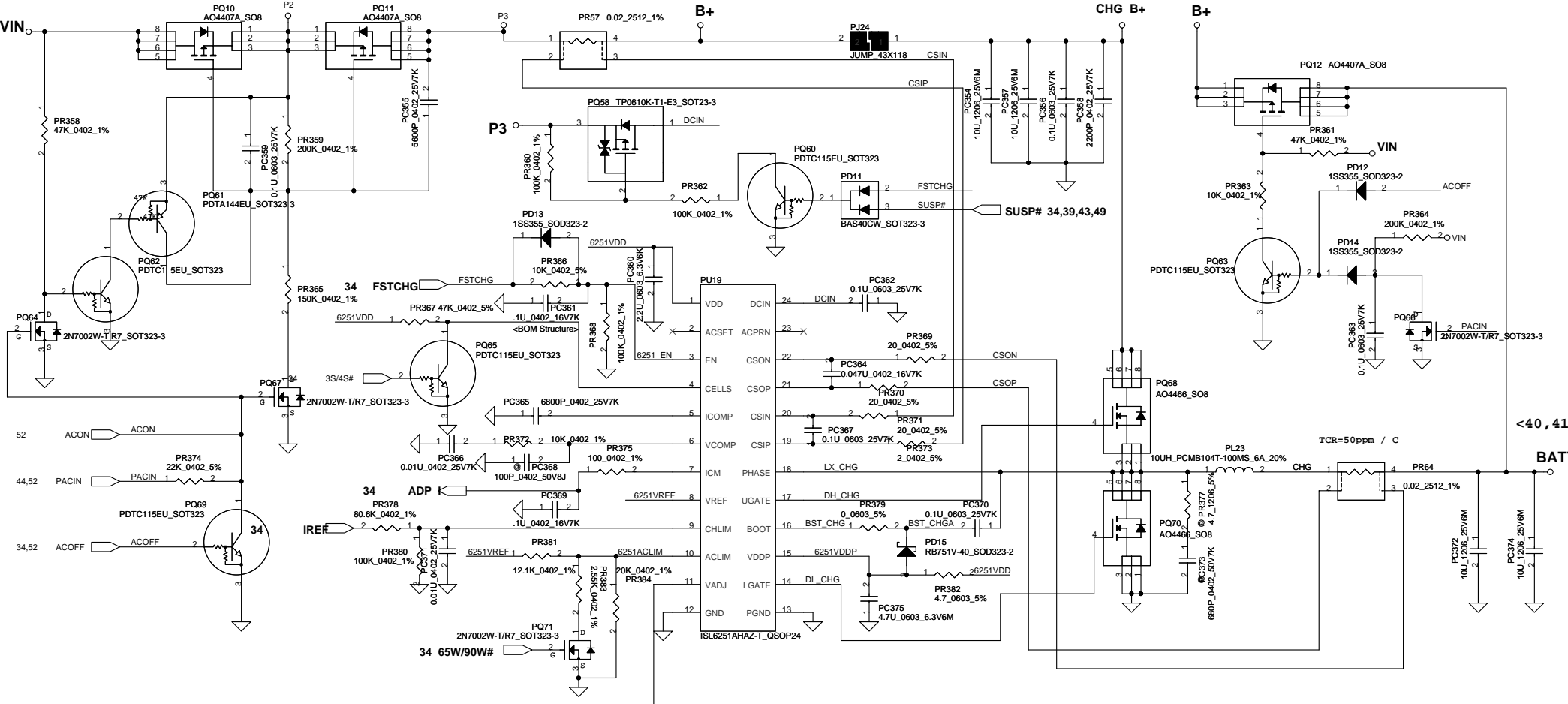


+3.3VALWP Ipeak=4.26A ; Then set I_{max}=4.26A
 Choke DCR_{max}=26.5m ohm, DCR_{typ}=23m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 316K)/10=158mV
 I_{limit}=158mV/(18m*1.2) ~ 158mV/15m
 =7.31A~10.53A
 I_{ocp}=I_{limit}+Delta I/2
 =7.76A~10.98A
 Delta I=0.908A (Freq=300KHz)

+5VALWP Ipeak=6.87A ; I_{max}=4.81A
 Choke DCR_{max}=26.5m ohm, DCR_{typ}=23m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 365K)/10=182.5mV
 I_{limit}=182.5mV/(18m*1.2) ~ 182.5mV/15m
 =8.44A ~ 12.16A
 I_{ocp}=I_{limit}+Delta I/2
 =8.90A ~ 12.62A
 Delta I=0.921A (Freq=400KHz)

check this part
 PD7
 1SS355_SOD323-2

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CP mode
 $I_{input} = (1/0.02) (0.05 * V_{aclm} / 2.39 + 0.05)$
 where $V_{aclm} = 1.502V$, $I_{input} = 4.07A$

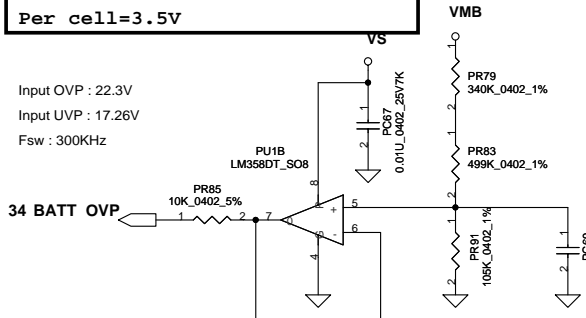
CC=0.6~4.48A
 $I_{ref} = 0.7224 * I_{charge}$
 $\Rightarrow K_i = 0.7224$
 $I_{REF} = 0.43V \sim 3.24V$

K_i
 $V_{chlim} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (155mV / PR369) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1 / 3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow K_i = 0.7224$

K_v
 $R_{internal} = 514K$ $R_{ec} = 3K$ $R_1 = PR379 = 15.4K$ $R_2 = PR381 = 31.6K$
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{cell} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * K_v = (4.2 - (4.2 + A * 0.175)) * K_v$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $K_v = 9.451$

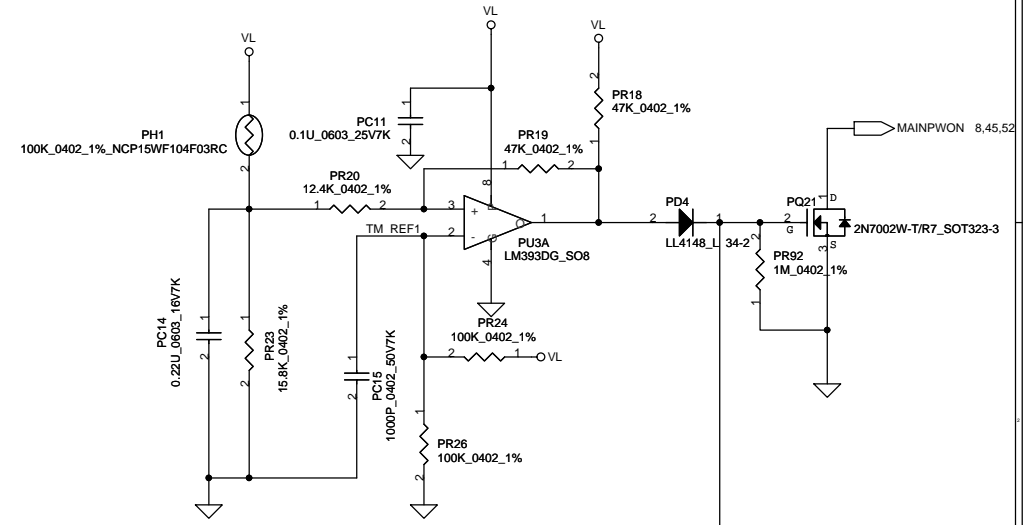
LI-3S :13.5V---BATT-OVP=2.007V
BATT-OVP=0.1487*VMB
Per cell=3.5V

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

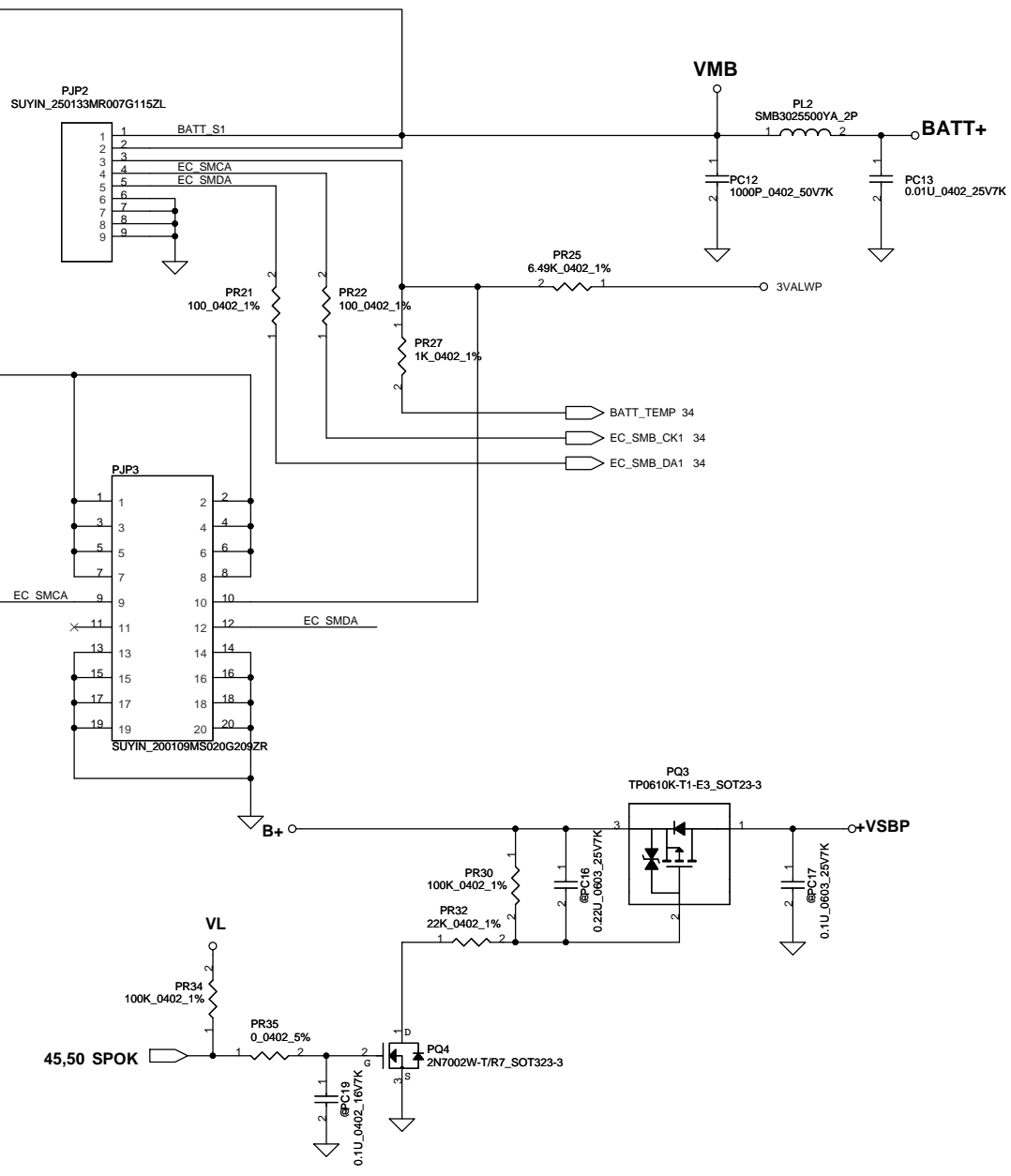
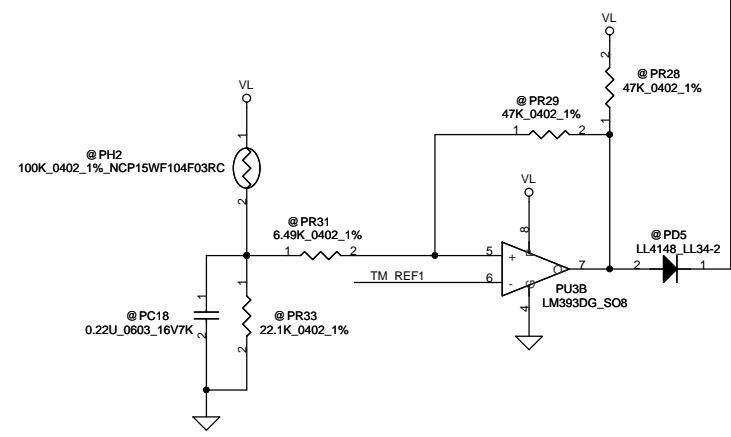


BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

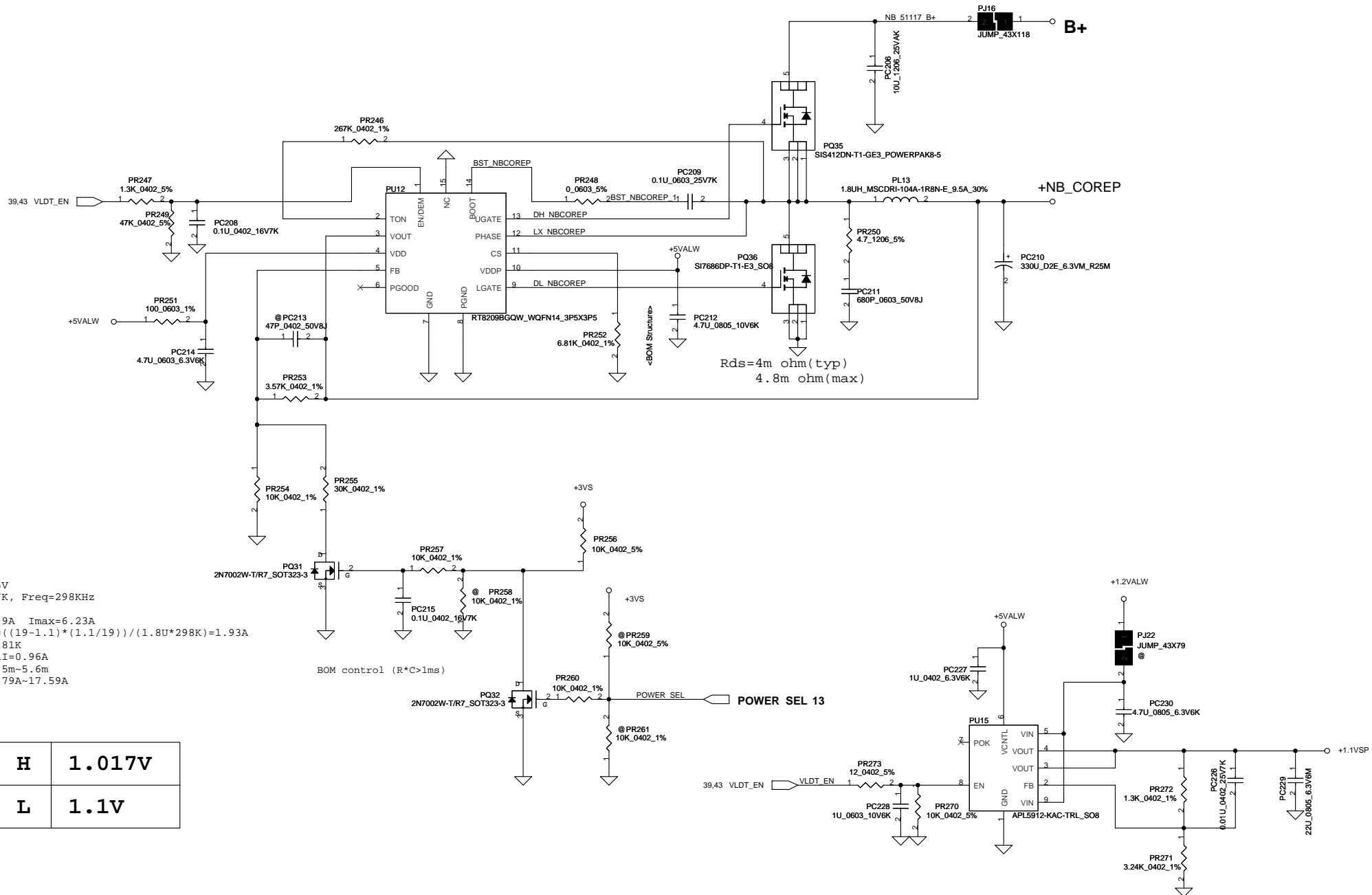
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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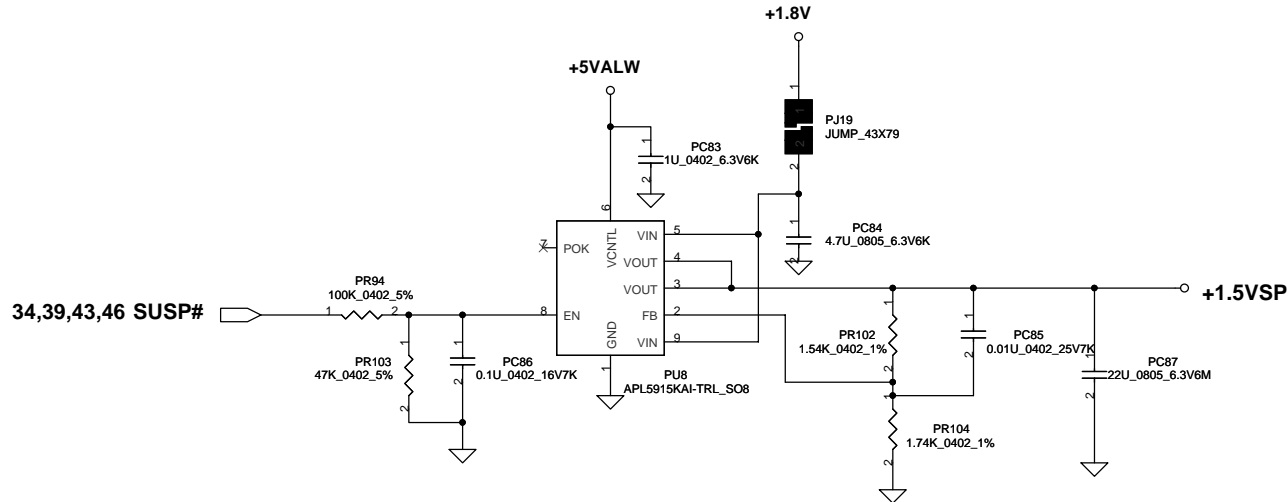
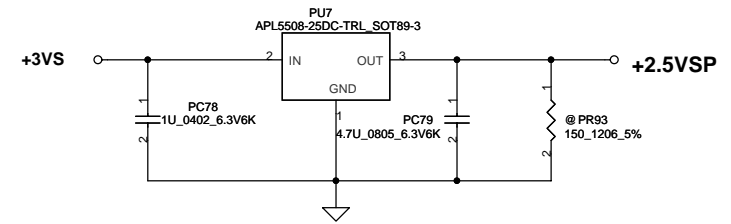
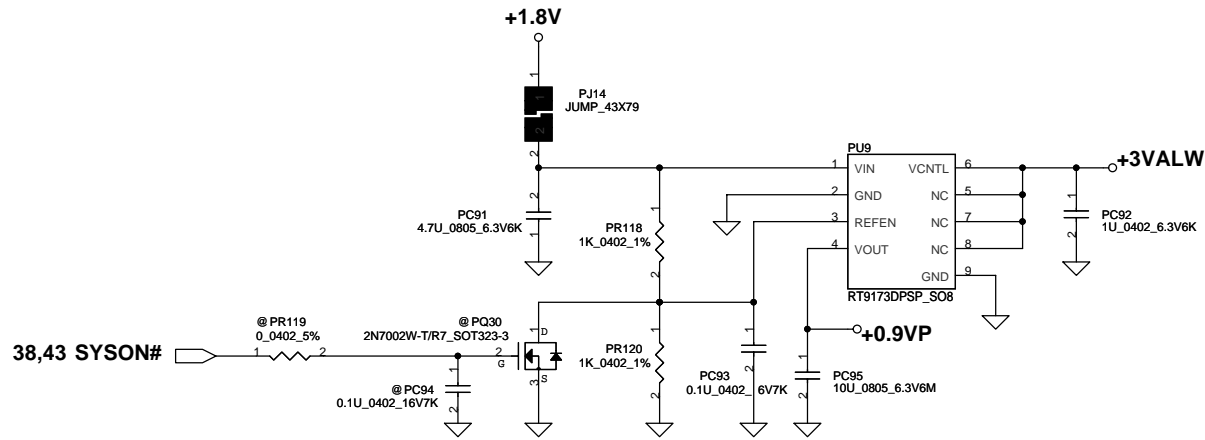


VFB=0.75V
 Rton=267K, Freq=298KHz

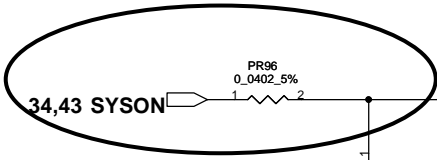
Ipeak=8.9A Imax=6.23A
 $\Delta I = ((19-1.1) * (1.1/19)) / (1.8U * 298K) = 1.93A$
 Rtrip=6.81K
 $1/2\Delta I = 0.96A$
 Rdson=4.5m~5.6m
 Iocp=10.79A~17.59A

BOM control (R*C>1ms)

H	1.017V
L	1.1V

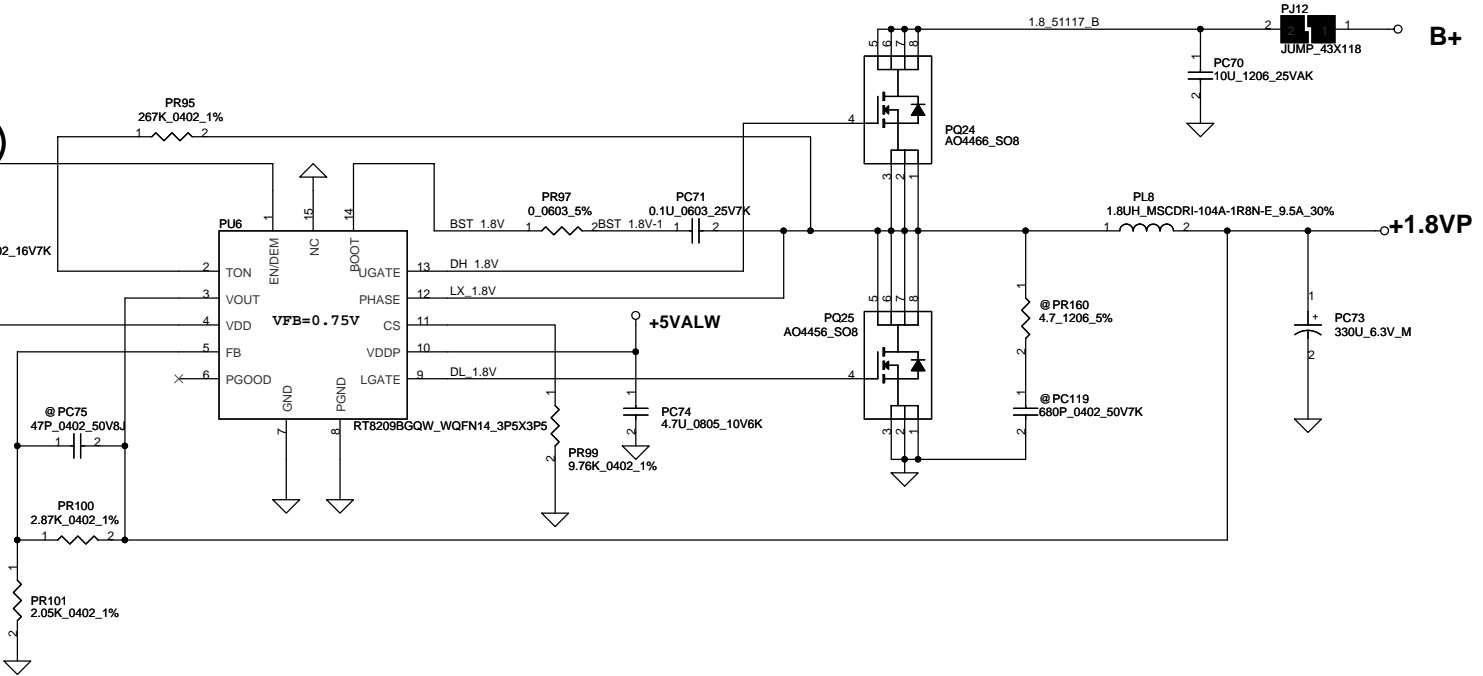


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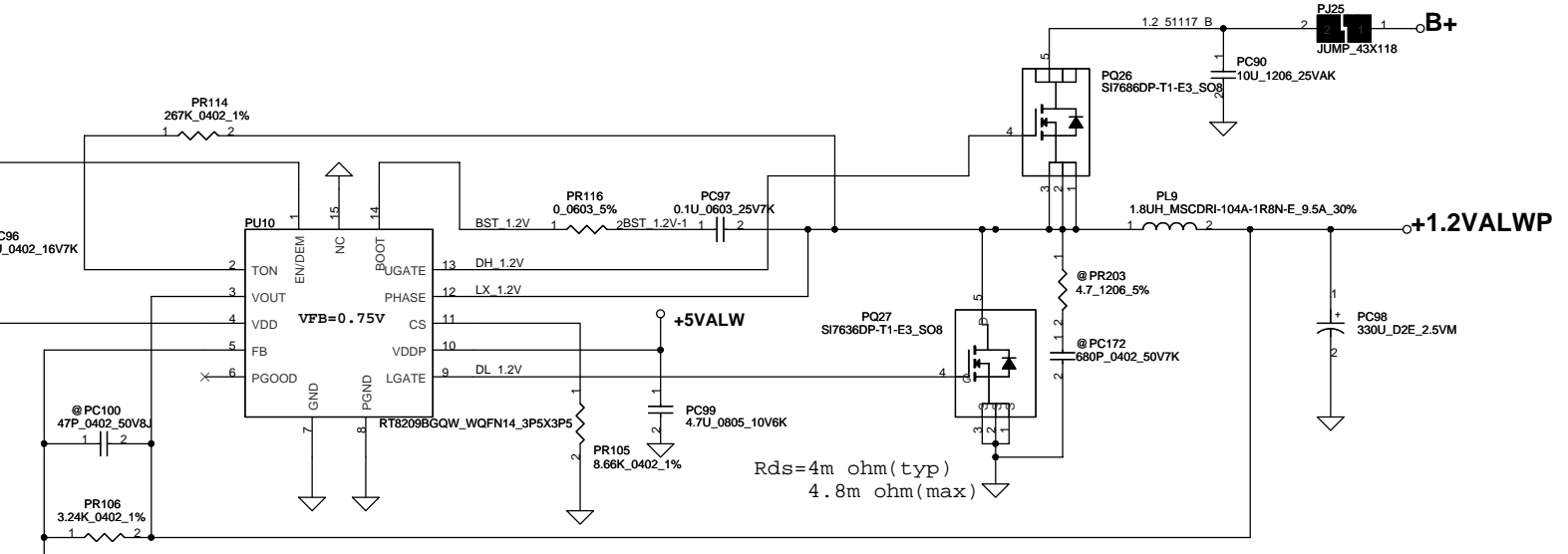
VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 297KHz$

Cout ESR=15m ohm
 $I_{peak} = 11.96A, I_{max} = 8.372A$
 $\Delta I = ((19-1.8) * (1.8/19)) / (L * F_{sw})$
 $((19-1.8) * (1.8/19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1/2 \Delta I = 1.524A$
 $R_{trip} = 9.76K$
 $I_{ocp} = 15.20A - 24.71A$



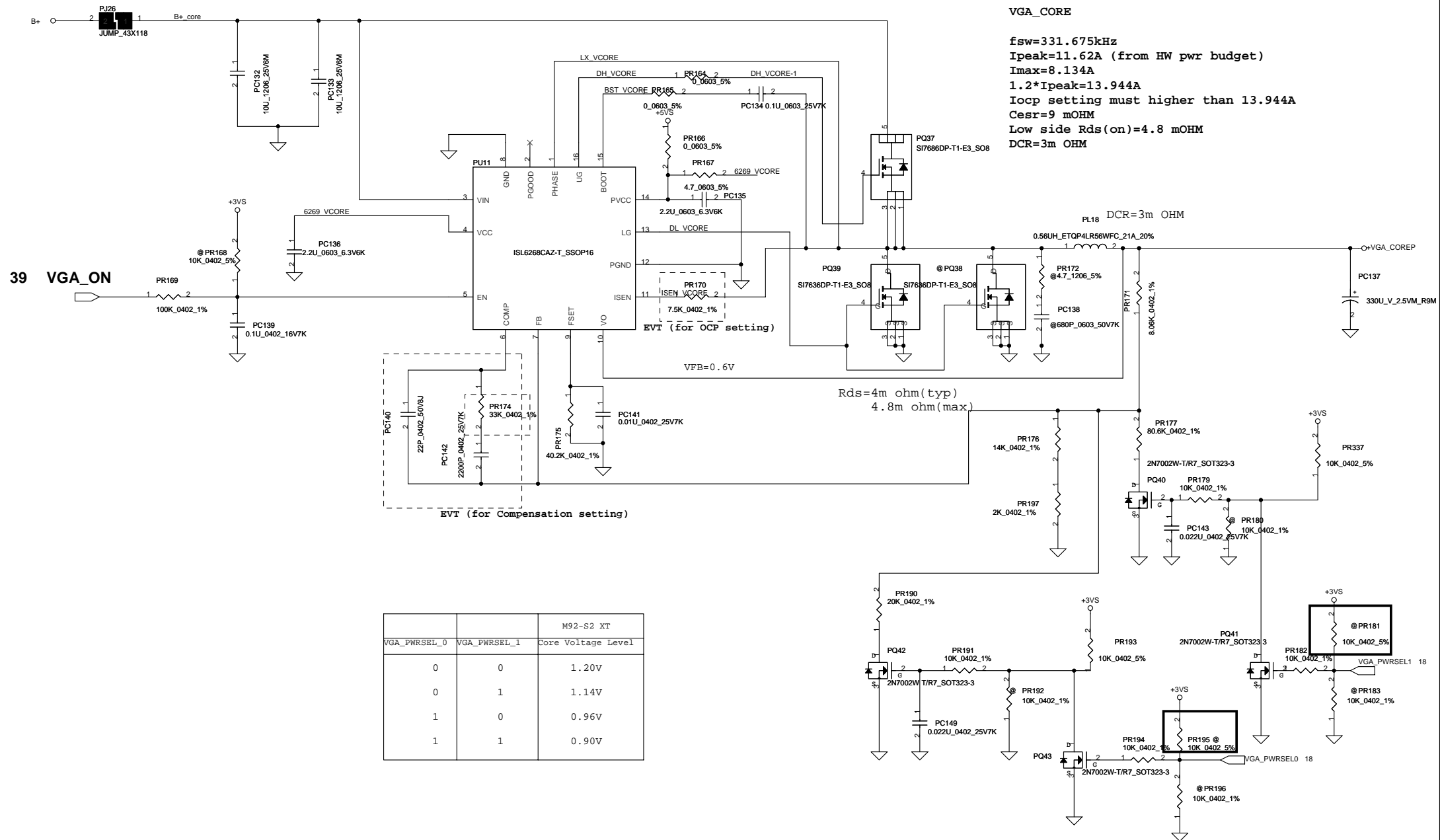
VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

1.2VP $I_{peak} = 7.4A ; I_{max} = 5.180A$
 $\Delta I = ((19-1.2) * (1.2/19)) / (L * F_{sw})$
 $((19-1.2) * (1.2/19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1/2 \Delta I = 1.05A$
 $R_{dson} = 15m / 18m \text{ ohm}$
 $set R_{trip} = 8.66K$
 $I_{ocp_min} = 4.77A$
 $I_{ocp_max} = 7.74A$



$R_{ds} = 4m \text{ ohm (typ)}$
 $4.8m \text{ ohm (max)}$

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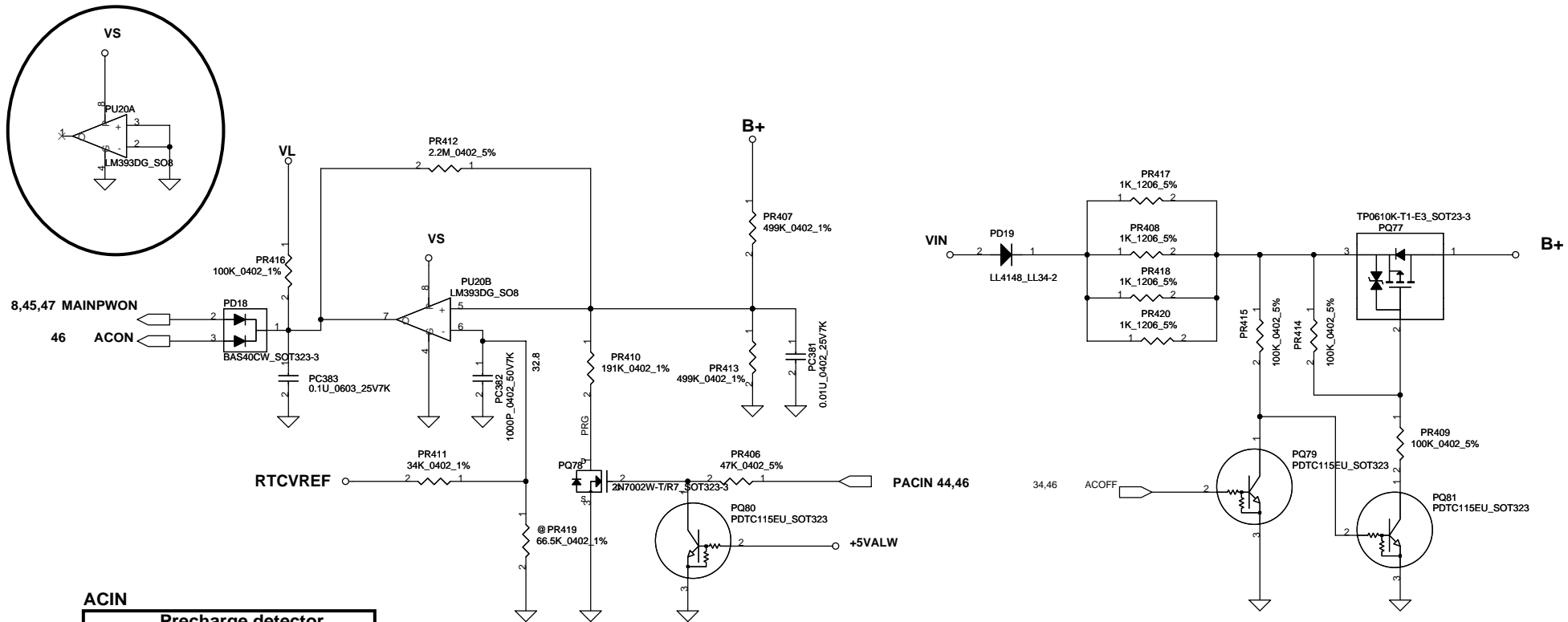


39 VGA_ON

VGA_CORE
 fsw=331.675kHz
 Ipeak=11.62A (from HW pwr budget)
 Imax=8.134A
 1.2*Ipeak=13.944A
 Iocp setting must higher than 13.944A
 Cesr=9 mOHM
 Low side Rds(on)=4.8 mOHM
 DCR=3m OHM

		M92-S2 XT
VGA_PWRSEL_0	VGA_PWRSEL_1	Core Voltage Level
0	0	1.20V
0	1	1.14V
1	0	0.96V
1	1	0.90V

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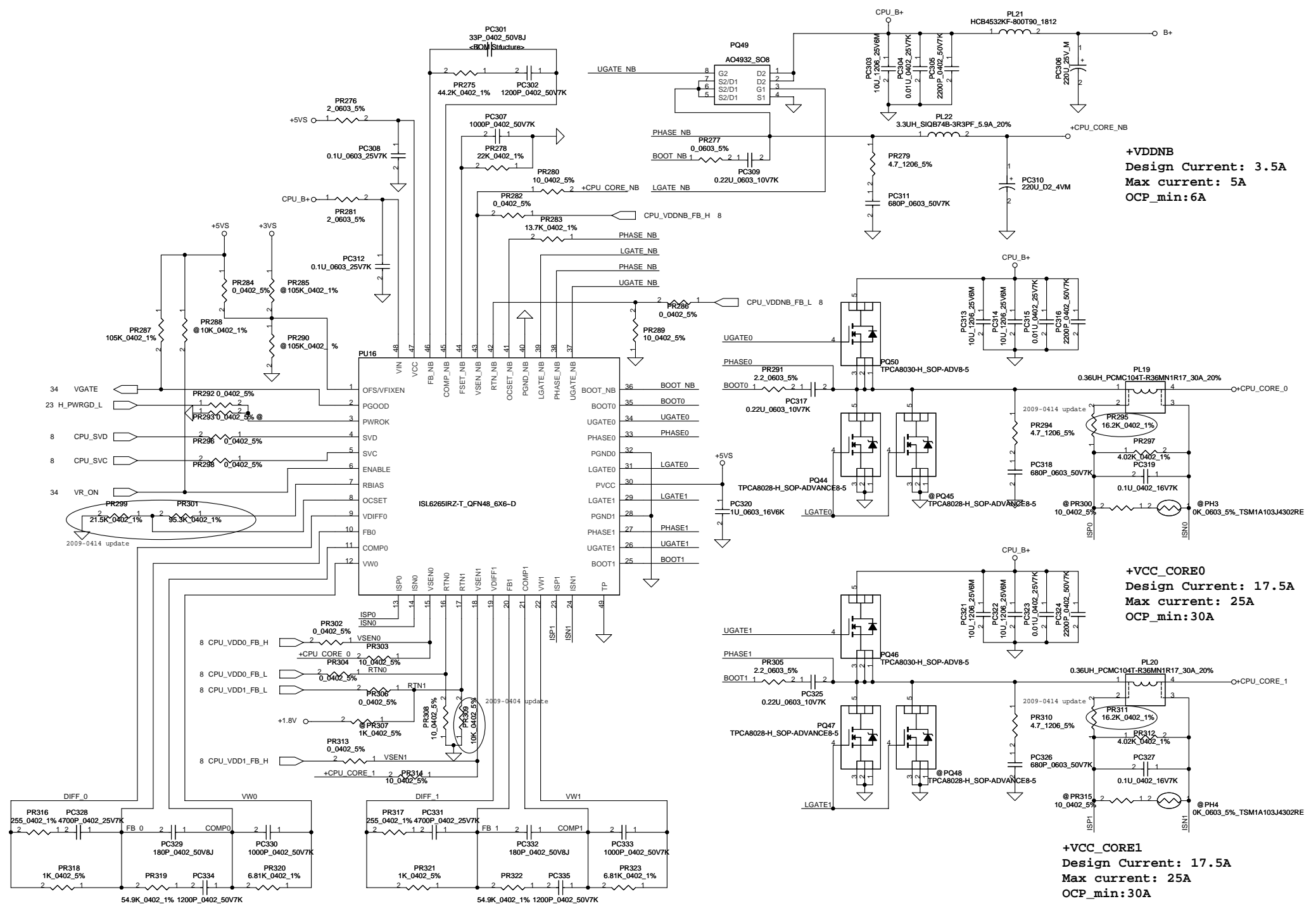
ACIN

Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be gitter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGA19331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
7							
8	Change Power Source	For WLAN wakeup	1.0	37	Change R550 to +3VALW	09, 05/07	Pre-MP
9							
10							
11							
12							
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Version change list (P.I.R. List) for HW

Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P 18	4/9	27				
3	BOM change	Change R178 R179 to 90 9/158 ohm	P 16	4/9	28				
4	BOM change	R30 R39 reserve	P 24	4/9	29				
5	BOM change	Add C30	P 38	4/9	30				
6	BOM change	Add R634 R639	P 28	4/9	31				
7	BOM change	C383 Reserve	P 24	4/9	32				
8		Pop R419	P 20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1 D2 Reserve pop R763	P 24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P 24	5/18					
12	Lid_SW intial issue	Add R19	P 28	5/18					
13	HPET timer issue	Change C288 C290 to 33P	P 16	5/18					
14	BOM change	change C276 C279 10P to 27P	P 19	5/19					
15									
16									
17									
18									
19									
20									
21									
22									
23									
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